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Design Closure Techniques

FPGA-DSGNCLOSURE (v1.0)

Course Specification

Course Description

Learn how to achieve design closure more efficiently and productively by using the three pillars of design closure (functional closure, timing closure, and power closure). Also learn how to solve functional behavior, timing, and power simultaneously to achieve faster time-to-market results.

The emphasis of this course is on:

- Defining what design closure is and describing the three pillars of design closure (functional closure, timing closure, and power closure)
- Using recommended coding techniques
- Applying initial design checks and reviewing timing summary and methodology reports for a design
- Using baselining to verify that a design meets timing goals and applying the guidelines described in the baselining process
- Performing quality of results (QoR) assessments at different stages to improve the QoR score
- Implementing Intelligent Design Runs (IDR) to automate analysis and timing closure for complex designs
- Applying common timing closure techniques
- Optimizing SLR crossings in Versal SSIT devices
- Reviewing the importance of power closure and device selection
- Estimating power consumption by using the Vivado™ Design Suite Power Report utility and performing power optimization on a design
- Identifying Versal™ adaptive SoC power and thermal solutions
- Utilizing architecture features to improve a design's power consumption

What's New for 2026.1

- Added a new module on using the AMD Ross™ agentic AI assistant for design closure using the Vivado Design Suite
- All labs have been updated to the latest software versions

Level – FPGA 2

Course Details

- 2 days ILT or 3 sessions 20261

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Course Part Number – FPGA-DSGNCLOSURE

Who Should Attend? – Software and hardware developers, system architects, and anyone who wants to learn about design closure techniques related to functional, timing, and power closure

Prerequisites

- Basic knowledge of FPGA and SoC architecture and HDL coding techniques
- Basic knowledge of the Vivado Design Suite

Software Tools

- Vivado Design Suite

Hardware

- Architecture: UltraScale™ FPGAs and Versal adaptive SoCs

After completing this comprehensive training, you will have the necessary skills to:

- Describe what design closure is as well as its three pillars
- Resolve setup and hold violations by reducing logic delay and net delay
- Improve clock skew and clock uncertainty
- Identify clock domain crossings (CDC) and scenarios that require synchronization circuits
- Perform QoR assessment at different stages and improve the QoR score
- Implement Intelligent Design Runs (IDR)
- Identify and apply common timing closure techniques
- Optimize SLR crossings in AMD Versal SSIT devices
- Apply the power closure flow for better time to market
- Leverage the Power Design Manager tool for power estimation
- Describe Versal adaptive SoC power and thermal solutions
- Perform power optimization on a design
- Utilize the AMD Ross agentic AI assistant to accelerate design closure

Course Outline

Day 1

Introduction

- **Introduction to Design Closure**
  Defines what design closure is and identifies the three pillars of design closure. {Lecture}

Functional Closure

- **HDL Coding Techniques**
  Covers basic digital coding guidelines used in an FPGA design. {Lecture}
- **Behavioral Simulation**
  Describes the process of behavioral simulation and the simulation options available in the Vivado IDE. {Lecture}

Timing Closure

- **Static Timing Analysis (STA)**
  Describes the clock and its attributes, basics of clock gating, and static timing analysis (STA). {Lecture}
- **UltraFast Design Methodology: Timing Closure**
  Provides an overview of the various stages of the UltraFast Design Methodology for timing closure. {Lecture}
- **Baselining**
  Demonstrates the performance baselining process, which is an iterative approach to incrementally constrain a design and meet timing. {Lecture, Lab}
- **Setup and Hold Violation Analysis**
  Covers what setup and hold slack are and describes how to perform input/output setup and hold analysis. {Lecture}
- **Reducing Logic Delay**
  Describes how to optimize regular fabric paths and paths with dedicated blocks and macro primitives. {Lecture}
- **Reducing Net Delay**
  Reviews different techniques to reduce congestion and net delay. {Lecture}
- **Improving Clock Skew**
  Describes how to apply various techniques to improve clock skew. {Lecture}
- **Improving Clock Uncertainty**
  Reviews various flows for improving clock uncertainty, including using parallel BUFGCE_DIV clock buffers, changing MMCM or

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PLL settings, and limiting synchronous clock domain crossing (CDC) paths. {Lecture, Lab}

- **QoR Reports Overview**
  Describes what quality of result (QoR) is and how to analyze the QoR reports generated by the Vivado IDE. {Lecture, Lab}

Day 2

Timing Closure (continued)

- **Clock Domain Crossing (CDC) and Synchronization Circuits**
  Explains what clock domain crossings (CDC) are and the scenarios that require synchronization circuits. {Lecture}
- **Intelligent Design Runs (IDR)**
  Introduces Intelligent Design Runs (IDR), which are special types of implementation runs that use a complex flow to attempt to close timing. {Lecture, Lab}
- **Versal Adaptive SoC: Timing Closure Techniques**
  Reviews the Advanced Flow for implementing Versal devices. Also covers common timing closure techniques for logic optimization, design analysis, timing closure and clock skew reduction. {Lecture}
- **Optimizing SLR Crossings in SSI Technology**
  Describe optimizing timing and design in Versal™ SSIT devices through efficient SLR crossings and constraints. {Lecture}

Power Closure

- **Understanding Design Power**
  Outlines the types of design power, describes the power closure flow, and identifies methods for bringing down the power of a device. {Lecture, Lab}
- **Versal Adaptive SoC: Power Design Manager**
  Discusses using the new Power Design Manager tool, including import and export functions. {Lecture, Lab}
- **Versal Adaptive SoC: Power and Thermal Solutions**
  Discusses the power domains in the Versal Adaptive SoC as well as power optimization and analysis techniques. Thermal design challenges are also covered. {Lecture}
- **Design Power Constraints**
  Describes what design power constraints are and how to use the Power Constraints Advisor tool. Power rail constraints are also covered. {Lecture}
- **Power Management Techniques**
  Identifies techniques used for low-power design. {Lecture}
- **Power Analysis and Optimization**
  Covers how to use report power commands to estimate power consumption. Also list the power estimation and analysis tools. {Lecture, Lab}

AI-assisted Design Closure

- **AMD Ross Agentic AI Assistant for Design Closure Using Vivado Design Suite**
  Introduces the AMD Ross agentic AI assistant, which uses natural language to analyze timing violations, suggest constraint fixes, and automate design closure workflows within the Vivado Design Suite. {Lecture}

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