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Designing with the Versal Adaptive SoC: Architecture

VER-ARCH (v1.0)

Course Specification

Course Description

Learn about the AMD Versal™ adaptive SoC architecture building blocks, such as the programmable logic, high-speed I/O, clocking, processing system, AI Engines, integrated networking solutions, and the programmable network on chip (NoC). Also learn how to use leading-edge memory and interfacing technologies to deliver powerful heterogeneous acceleration for any application.

The emphasis of this course is on:

- Reviewing the architecture of the Versal adaptive SoC
- Describing the architectures and key features of Versal Premium Series Gen 2 and Versal RF Series devices
- Describing the different compute resources available in the Versal architecture
- Describing the architectures of the network on chip (NoC) and AI Engine
- Outlining the memory solutions and programming interfaces available in the Versal adaptive SoC
- Identifying the integrated networking solutions available in the Versal adaptive SoC
- Identifying the PCI Express® and serial transceiver solutions available in the Versal adaptive SoC

What's New for 2026.1

- Added new modules:
  - AMD Versal Premium Series Gen 2: Architecture Overview
  - AMD Versal RF: Architecture Overview
  - AMD Versal Adaptive SoC: Networking IPs
- Design Tool Flow module: Introduced the Vitis™ AI development flow and the Neural Processing Unit (NPU)
- Processing System module: Updated Versal APU configuration details based on the selected Versal device
- Boot and Configuration module: Added information on DFX + Segmented Configuration support
- DSP Engine module: Added DSP58 performance, migration, and Vivado™ feature-access information
- NoC Introduction and Concepts module: Introduced the latest Vivado Design Suite features for NoC development
- PCI Express® module: Added Versal Premium Series Gen 2 CPM6, CXL overview, and key CPM6 controller features
- All labs have been updated to the latest software versions

Level – VER 1

Course Details

- 2 days ILT or 3 sessions/19

Course Part Number – VER-ARCH

Who Should Attend? – Software and hardware developers, system architects, DSP users, and anyone who wants to learn about the architecture of the Versal adaptive SoC

Prerequisites

- Basic knowledge of AMD FPGAs and adaptive SoCs
- Basic knowledge of the Vivado™ and Vitis™ tools

Software Tools

- Vivado Design Suite 2026.1
- Vitis unified software platform 2026.1

Hardware

- Architecture: Versal adaptive SoC
- Demo board: Versal VCK190 Evaluation Platform

After completing this comprehensive training, you will have the necessary skills to:

- Describe the AMD Versal adaptive SoC architecture
- Describe the architectures and key features of Versal Premium Series Gen 2 and Versal RF Series devices
- Identify the different compute resources available in the Versal devices
- Utilize the hardened blocks available in the Versal architecture
- Describe the NoC and AI Engine architectures
- Outline the memory solutions and programming interfaces available in the Versal adaptive SoC
- Identify the integrated networking solutions available in the Versal adaptive SoC
- Identify the PCI Express and serial transceiver solutions available in the Versal adaptive SoC

Course Outline

Day 1

- **Introduction and Portfolio Overview**
  Describes the need for Versal devices and offers an overview of the Versal portfolio. {Lecture}
- **Architecture Overview**
  Provides a high-level overview of the Versal architecture, illustrating the various compute resources available in the Versal architecture. {Lecture}
- **Versal Premium Series Gen 2: Architecture Overview**
  Describes the AMD Versal Premium Series Gen 2 architecture, including key architectural blocks, major enhancements, and Memory on Package (MoP) device features and benefits. {Lecture}
- **Versal RF: Architecture Overview**
  Reviews the AMD Versal RF Series architecture, including key architectural blocks, RF data converter solutions, and DSP hard IP capabilities. {Lecture}
- **Design Tool Flow**
  Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture, Lab}
- **Programmable Logic (PL)**
  Describes the logic resources available in the programmable logic. {Lecture}
- **SelectIO Resources**
  Describes the I/O bank, SelectIO™ interface, and I/O delay features. {Lecture}
- **Clocking Architecture**
  Discusses the clocking architecture, clock buffers, clock routing, clock management functions, and clock de-skewing options. {Lecture, Lab}
- **Processing System**
  Reviews the Arm® Cortex® APUs and RPUs that form the processing system. The platform management controller (PMC), processing system manager (PSM), I/O peripherals, and PS-PL interfaces are also covered. {Lecture}
- **Platform Management Controller (PMC)**

Describes the platform management controller architecture and the role of platform loader and manager (PLM) in the Versal device boot process. {Lecture}

- **Boot and Configuration**

  Covers the boot phases, flows, and modes along with the process of generating a boot image. Also discusses the concept and benefits of segmented configuration. {Lecture, Lab}

Day 2

- **System Interrupts**

  Discusses the different system interrupts and interrupt controllers. {Lecture}

- **Timers, Counters, and RTC**

  Provides an overview of timers and counters, including the system counter, triple timer counter (TTC), watchdog timer, and real-time clock (RTC). {Lecture}

- **DSP Engine**

  Describes the DSP58 slice and compares the DSP58 slice with the DSP48 slice. DSP58 modes and applications are also covered in detail. {Lecture, Lab}

- **AI Engine**

  Discusses the AI Engine array architectures (AIE, AIE-ML, and AIE-ML v2), terminology, and AIE interfaces. Also lists the key differences between the AIE, AIE-ML, and AIE-ML v2 architectures. {Lecture, Lab}

- **NoC Introduction and Concepts**

  Covers the reasons to use the network on chip, its basic elements, design entry flows, and common terminology. {Lecture, Lab}

- **Memory Solutions**

  Describes the available memory resources, such as block RAM, UltraRAM, LUTRAM, embedded memory, OCM, and DDR. The integrated memory controllers are also covered. {Lecture}

- **Programming Interfaces**

  Reviews the various programming interfaces in the Versal device. {Lecture}

- **Networking IPs**

  Outlines the integrated networking IP available in Versal devices, including the MRMAC, DCMAC, 600G Interlaken with FEC, and HSC subsystems. {Lecture}

- **PCI Express**

  Provides an overview of the PCIe module and describes the PL and CPM PCIe blocks. {Lecture, Lab}

- **Serial Transceivers**

  Describes the transceivers in the Versal device. Also introduces the new GT Wizard Subsystem flow. {Lecture, Lab}