

Course Description

Learn about the AMD Versal™ AI Edge Series Gen 2 and Prime Series Gen 2 adaptive SoC architectures, which combine programmable logic with a new high-performance processing system and next-generation AI Engines. Also learn how these devices facilitate end-to-end acceleration and maximize system performance for embedded systems—all in a single device built on a foundation of enhanced safety and security.

The emphasis of this course is on:

- Describing the different compute resources available in the Versal adaptive SoC
- Explaining the new high-performance processing system (PS)
- Describing the next-generation AI Engine architecture
- Describing the network on chip (NoC) resources
- Outlining the available DDR5/LPDDR5X memory controller support
- Reviewing the new image and video processing hard blocks
- Explaining the functional safety and security enhancements
- Identifying the available PCI Express® Gen 5 and 32G high-speed serial transceiver solutions

What's New for 2026.1

- Design Tool Flow module: Introduced the Vitis™ AI development flow and the Neural Processing Unit (NPU)
- Processing System (PS) module: Updated the Versal processing system feature comparison table
- Boot and Configuration module: Added information on DFX + Segmented Configuration support
- Designing with DDR5 module: Added auto-precharge and write-order control to memory performance factors
- Added new module: AMD Vitis AI for AMD Versal AI Edge Series Gen 2 Devices
- All labs have been updated to the latest software versions

Level – VER 1

Course Details

- 2 days ILT or 3 sessions/19
- Course Part Number** – VER2-ARCH

Who Should Attend? – Software and hardware developers, system architects, and anyone who wants to learn about the architecture of the Versal AI Edge Series Gen 2 and Prime Series Gen 2 devices

Prerequisites

- Basic knowledge of AMD FPGAs and adaptive SoCs
- Basic knowledge of the AMD Vivado™ and Vitis™ tools

Software Tools

- Vivado Design Suite 2026.1
- Vitis Unified IDE 2026.1

Hardware

- Architecture: Versal adaptive SoC

After completing this comprehensive training, you will have the necessary skills to:

- Describe the different compute resources available in the AMD Versal adaptive SoC
- Explain the new high-performance processing system (PS)
- Describe the next-generation AI Engine architecture
- Describe the programmable network on chip (NoC) resources

- Outline the available DDR5/LPDDR5X memory controller support
- Describe the new image and video processing hard blocks
- Explain the functional safety and security enhancements
- Identify the available PCI Express Gen 5 and 32G high-speed serial transceiver solutions

Course Outline

Day 1

Introduction and Portfolio Overview

Describes the need for Versal devices and offers an overview of the Versal portfolio. {Lecture}

Architecture Overview

Provides a high-level overview of the Versal architecture, illustrating the various compute resources available in the Versal architecture. {Lecture}

Design Tool Flow

Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture, Lab}

Programmable Logic (PL)

Describes the logic resources available in the programmable logic. Also discusses the clocking architecture, clock buffers, clock routing, and clock de-skewing options. {Lecture}

SelectIO™ Resources

Describes the I/O bank, SelectIO interface, and I/O delay features. {Lecture}

Processing System

Reviews the Arm® Cortex®-A78AE processor APU and Cortex-R52 processor RPU that form the processing system. Discusses high-speed connectivity, boot modes, system peripherals, and power domains. Also introduces the AMD Embedded Development Framework (EDF) for streamlined application development. {Lecture, Lab}

Platform Management Controller (PMC)

Describes the platform management controller architecture and the role of platform loader and manager (PLM) in the Versal device boot process. {Lecture}

Boot and Configuration

Covers the boot phases, flows, and modes along with the process of generating a boot image. Also discusses the concept and benefits of segmented configuration. {Lecture}

AIE-ML v2 Architecture Overview

Discusses the AI Engine AIE-ML v2 array architecture and its tiles. Also lists the key differences between the AIE, AIE-ML, and AIE-ML v2 architectures. {Lecture, Lab}

Day 2

AMD Vitis AI for AMD Versal AI Edge Series Gen 2 Devices

Describes the Vitis AI software stack, AI deployment flow, and NPU optimization capabilities for AMD Versal AI Edge Series Gen 2 devices. {Lecture}

NoC Architecture

Covers the reasons to use the network on chip, the NoC architecture and its basic elements, design entry flows, and common terminology. {Lecture}

Designing with DDR5

Describes the DDR5 memory controller features and its configuration flow. Also demonstrates how to tune a design to increase efficiency. {Lecture, Lab}

- **Multimedia Hard Blocks**

Reviews the multimedia-specific hard IP blocks such as VCU2, GPU, and ISP available in the Versal devices. {Lecture, Lab}

- **Security and Functional Safety Overview**

Describes the security architecture and the available security units. Also provides an overview of the increased embedded system security. {Lecture}

- **PCI Express Solutions**

Provides an overview of the PCIe® module and describes the PL and MDB PCIe blocks. {Lecture, Lab}

- **Serial Transceivers**

Describes the transceivers in the Versal device. Also introduces the new GT Wizard Subsystem flow. {Lecture, Lab}