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Vitis Model Composer: A MATLAB and Simulink-based Product

DSP-MCSIM (v1.0)

Course Specification

Course Description

This course provides experience with using the AMD Vitis™ Model Composer tool for model-based designs.

The course provides experience with:

- Creating a model-based design using HDL, HLS, and AI Engine library blocks along with custom blocks in Vitis Model Composer
- Implementing DSP functions using Vitis Model Composer
- Utilizing design implementation tools
- Transforming algorithmic specifications to production-quality IP implementations using automatic optimizations and leveraging the high-level synthesis technology of the Vitis Unified IDE
- Creating Versal™ AI Engine graphs and kernels using Vitis Model Composer
- Connecting AI Engine blocks and non-AI Engine blocks
- Verifying and debugging AI Engine code using the Analysis view of the Vitis Unified IDE
- Simulating and debugging a complex system created using AI Engine library blocks
- Performing hardware validation using Vitis Model Composer
- Integrating an AI Engine design from Vitis Model Composer into the Vitis Unified IDE

What's New for 2025.2

- Block in the Basics of the Simulink® Environment module: Updated information on using the Scope block
- Compilation and Hardware Co-Simulation module: Added information on the Vitis Subsystem (VSS) export type from the HDL library
- All labs have been updated to the latest software versions

Level – DSP 3

Course Details

- 2 days ILT or 3 sessions/19

Course Part Number – DSP-MCSIM

Who Should Attend? – System engineers, system designers, logic designers, and experienced hardware engineers who are implementing Versal AI Engine, HDL, and HLS algorithms using the MathWorks MATLAB® and Simulink® software and want to use Vitis Model Composer

Prerequisites

- Basic experience with the MATLAB and Simulink software
- Basic understanding of DSP designs and sampling theory
- Comfort with the C/C++ programming language for HLS or AI Engine model designs

Software Tools

- Vivado Design Suite 2025.2
- Vitis Unified IDE 2025.2
- MATLAB with Simulink software R2025b

Hardware

- Architecture: Zynq™ UltraScale+™ MPSoC and Versal™ AI Core series
- Demo board: Versal VCK190 Evaluation Platform*

* This course focuses on the Zynq UltraScale+ and Versal architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab environment or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use optimized HDL, HLS, and AI Engine blocks directly from the Simulink tool library browser
- Create, simulate, and debug a Vitis Model Composer design in the Simulink environment using HDL, HLS, and AI Engine block libraries
- Perform co-simulation and hardware verification
- Use DSP blocks in Vitis Model Composer to implement DSP functions
- Implement multi-rate systems in Vitis Model Composer
- Design a processor-controllable interface using Vitis Model Composer
- Generate IPs from C-based design sources using Vitis HLS for use in the Vitis Model Composer environment
- Import custom HDL, HLS, and AI Engines code as blocks into Vitis Model Composer
- Generate output products using automatic code generation
- Connect AI Engine blocks and non-AI Engine blocks
- Perform AI Engine code verification using the Analysis view of the Vitis Unified IDE
- Create, simulate, and debug a complex system created using AI Engine library blocks
- Validate an AI Engine design using hardware emulation
- Integrate an AI Engine design from Vitis Model Composer into the Vitis Unified IDE

Course Outline

Day 1

Introduction to Vitis Model Composer

- **Introduction to Vitis Model Composer**
  Introduces the Vitis Model Composer tool and describe the optimized HDL, HLS, and AI Engine library blocks available in Vitis Model Composer. {Lecture}
- **Basics of the Simulink Environment**
  Describes the Simulink software environment, some of the commonly used signal source and sink blocks available in the Simulink software, and how hierarchical designs are created and protected using masked subsystems. {Lecture, Lab}

Vitis Model Composer for HDL

- **HDL Library in Vitis Model Composer**
  Illustrates how the HDL library can be used in Vitis Model Composer and how to analyze performance and resource usage in Vitis Model Composer. {Lecture, Labs}
- **HDL Library Compilation and Hardware Co-Simulation**
  Covers how to import HDL modules as well as perform HDL co-simulation and hardware verification. Reviews the compilation types for Vitis Model Composer designs. Also introduces Super Sample Rate (SSR) blocks in Vitis Model Composer. {Lecture}
- **DSP Blocks in Vitis Model Composer**
  Describes the DSP blocks in the HDL and AI Engine library. Also reviews the basics of AXI4 interfaces. {Lecture, Lab}

- **Working with Filter Designs**
  Describes the concept of designing filters supported by Vitis Model Composer. {Lecture, Lab}
- **Working with Multi-Rate Systems**
  Explains how a multi-rate DSP system uses multiple sampling rates within a system. {Lecture}

Day 2

Vitis Model Composer for HLS

- **HLS Library in Vitis Model Composer**
  Describes how to create Vitis Model Composer designs using HLS block libraries, import C/C++ code into Vitis Model Composer, and generate output products using automatic code generation. {Lecture, Labs}

Vitis Model Composer for AI Engines

- **AI Engine Library in Vitis Model Composer**
  Demonstrates the usage the AI Engine library in Vitis Model composer for creating an AI Engine design, which involves preparing the kernel and importing the AI Engine code as a block. {Lecture}
- **AI Engine Simulation and Code Generation**
  Illustrates the process of generating AI Engine code with a data flow graph, which involves Simulink simulation with the AI Engine library for functional verification. Also describe the hardware validation flow through generating a hardware image targeting a specific platform for the Simulink environment. {Lecture, Labs}
- **Connecting AI Engine and Non-AI Engine Blocks**
  Explains how to interconnect AI Engine blocks and non-AI Engine (HDL and HLS) blocks. {Lecture}
- **Analyzing and Debugging an AI Engine Design in Vitis Model Composer**
  Explain the Versal AI Engine code verification process and how to use the analyzer, Vitis debugger, and data inspector to debug the AI Engine design. {Lecture, Lab}
- **Exporting an AI Engine Design to the Vitis Unified IDE**
  Demonstrates how to export an AI Engine design into the Vitis Unified IDE after it has been simulated and validated in Vitis Model Composer. {Lab}

GitHub Examples

- **Exploring Vitis Model Composer Examples in GitHub**
  Introduces different categories of Vitis Model Composer examples in GitHub and describes the methods to access these examples from GitHub. {Lecture}