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# UltraFast Design Methodology

FPGA-VDM (v1.0)

**Course Specification**

## Course Description

Learn how to improve design speed and reliability by using the UltraFast™ Design Methodology and the Vivado™ Design Suite.

The focus is on:

- Optimizing system reset design and synchronization circuits
- Employing best practice HDL coding techniques
- Applying appropriate timing closure techniques
- Reviewing an UltraFast Design Methodology case study

**What's New for 2025.2**

- All labs have been updated to the latest software versions

**Level** – FPGA 3

**Course Details**

- 2 days ILT or 3 sessions

**Course Part Number** – FPGA-VDM

**Who Should Attend?** – Engineers who seek training for FPGA design best practices that increase design performance and increase development productivity.

**Prerequisites**

- Basic HDL knowledge (VHDL or Verilog)
- Digital design knowledge and experience

**Software Tools**

- Vivado Design Suite 2025.2

**Hardware**

- Architecture: UltraScale™ FPGAs*
- Demo board: None*

* This course focuses on the UltraScale architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the UltraFast design methodology checklist
- Identify key areas to optimize your design to meet your design goals and performance objectives
- Define a properly constrained design
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
- Build resets into your system for optimum reliability and design speed
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Identify timing closure techniques using the Vivado Design Suite
- Describe how the UltraFast design methodology techniques work effectively through case studies and lab experience

## Course Outline

**Day 1**

**UltraFast Design Methodology – Planning**

- **UltraFast Design Methodology: Introduction**
  Introduces the UltraFast Design Methodology and the UltraFast Design Methodology checklist. {Lecture}
- **UltraFast Design Methodology: Board and Device Planning**
  Introduces the methodology guidelines on board and device planning. {Lecture}
- **Vivado Design Suite I/O Pin Planning**
  Describes the I/O Pin Planning layout for performing pin assignments in a design. {Lecture, Lab}
- **Power Estimation Using XPE**
  Illustrates estimating the amount of resources and default activity rates for a design and evaluating the estimated power calculated by XPE. {Lecture, Lab}

**UltraFast Design Methodology – Design Creation**

- **UltraFast Design Methodology: Design Creation**
  Introduces the UltraFast methodology guidelines on design creation. {Lecture}
- **RTL Development**
  Covers RTL and the RTL design flow, recommended coding guidelines, using control signals, and recommendations on resets. {Lecture}
- **Resets**
  Investigates the impact of using asynchronous resets in a design. {Lecture, Lab}
- **Pipelining**
  Demonstrates the use of pipelining to improve design performance. {Lecture, Lab}
- **Synchronous Design Techniques**
  Introduces the synchronous design techniques used in an FPGA design. {Lecture}

**Vivado IP Flow**

- **Getting Started with Vivado IP Integrator**
  Introduces the Vivado IP integrator tool and its features. Also reviews creating and working with block designs. {Lecture, Lab}
- **Designing IP Subsystems Using Vivado IP Integrator**
  Illustrates designing with processor-based subsystems and working with custom RTL code. Also explains how to create Vitis™ platforms using Vivado IP integrator. {Lecture}
- **Creating and Packaging Custom IP**
  Covers creating your own IP and package and including it in the Vivado IP catalog. {Lecture}

**Version Control Systems**

- **Revision Control Systems in the Vivado Design Suite**
  Reviews using version control systems with Vivado IDE design flows. {Lecture}

**Day 2**

**UltraFast Design Methodology – Implementation**

- **UltraFast Design Methodology: Implementation**
  Introduces the methodology guidelines on implementation. {Lecture}
- **Incremental Compile Flow**
  Discusses the incremental compile flow last-minute RTL changes are made. {Lecture}

**UltraFast Design Methodology – Design Analysis**

- **UltraFast Design Methodology: Timing Closure**
  Introduces the UltraFast methodology guidelines on timing closure. {Lecture}
- **Introduction to Vivado Reports**
  Demonstrates generating and using Vivado timing reports to analyze failed timing paths. {Lecture, Demo}
- **Baselining**
  Illustrates how to apply recommended baselining procedures to progressively meet timing closure. {Lecture, Lab}
- **Clock Domain Crossing and Synchronization Circuits**
  Outlines using synchronization circuits for clock domain crossings. {Lecture}
- **QoR Reports Overview**
  Describes what quality of result (QoR) is and how to analyze the QoR reports generated by the Vivado IDE. {Lecture, Lab}
- **Timing Closure Using Physical Optimization Techniques**
  Show how to use physical optimization techniques for timing closure. {Lecture, Lab}
- **Power Management Techniques**
  Identifies the techniques used for low power design. {Lecture}

**Floorplanning**

- **Introduction to Floorplanning**
  Provides an introduction to floorplanning and how to use Pblocks while floorplanning. {Lecture}
- **Congestion**
  Describes congestion and addresses congestion issues. {Lecture}

**Debugging**

- **Vivado Design Suite Debug Methodology**
  Covers debug core recommendations and employ the debug methodology for debugging a design using the Vivado logic analyzer. {Lecture}