AMD
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Designing with the Versal Adaptive SoC: Serial Transceivers

VER-TRX (v1.0)

Course Specification

Course Description

This course provides a system-level understanding of AMD Versal™ adaptive SoC serial transceivers. Transceiver architecture, IP generation, simulation, and implementation are covered. Additional information on PCB design issues is also covered.

The focus is on:

- Constructing a system using Versal device serial transceivers by:
  - Selecting the appropriate IP for an application
  - Configuring Transceivers Wizard IPs
  - Using transceiver IP example designs
  - Simulating and implementing transceiver IPs
- Identifying the advanced capabilities of the serial transceivers, including using IBERT and eye scan options
- Accessing the appropriate reference material for board design issues involving signal integrity, the power supply, reference clocking, and trace design

What's New for 2025.2

- New module on Versal Transceiver design flow
- All labs have been updated to the latest software versions

Level – VER 3

Course Details

- 1 day ILT or 2 sessions/9
- 1**Course Part Number** – VER-TRX

Who Should Attend?

- Hardware designers who want to create applications using serial transceivers
- System architects who want to leverage the key advantages of serial transceivers

Prerequisites

- Knowledge of Verilog or VHDL
- Familiarity with logic design (state machines and synchronous design)
- Some experience with AMD Vivado™ implementation
- Some experience with a simulation tool, preferably the Vivado simulator
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

Software Tools

- Vivado Design Suite 2025.2

Hardware

- Architecture: All Versal adaptive SoC devices
- Evaluation board:
  - GTY users: Versal VCK190 board
  - GTM users: Versal VPK120 board

After completing this comprehensive training, you will have the necessary skills to:

- Describe and utilize the building blocks of the serial transceivers in the AMD Versal devices
- Describe and utilize the ports and attributes of the transceivers
- Design, simulate, and implement the transceivers
- Utilize transceiver debugging options
- Identify transceiver use cases
- Describe transceiver board design requirements

Course Outline

Day 1

- **Course Introduction**
  Introduces the course and discusses serial transmission. {Lecture}
- **GTY/GTYP Transceiver Shared Features**
  Describes the structure and shared features, such as clocking and reset schemes, of the Versal device serial transceivers. {Lecture}
- **GTY/GTYP Transceiver Architecture**
  Discusses the architecture and functionality of the transmit and receive functional blocks. {Lecture}
- **Transceiver Design Flow**
  Discusses options to generate transceiver IPs. {Lecture}
- **Transceiver IP Generation**
  Demonstrates usage of the Transceivers Wizard. {Lecture, Lab}
- **Transceiver IP Simulation**
  Covers how to perform transceiver design simulation. {Lecture, Lab}
- **Transceiver IP Implementation**
  Illustrates how to perform transceiver implementation and verification on real hardware. {Lecture, Lab targeting the VCK190 board}
- **Transceiver Use Cases**
  Discusses using the transceivers for several protocol applications, including the PCI Express®, Ethernet, Interlaken, JESD204, and Aurora interfaces. {Lecture}
- **Transceiver Board Design**
  Describes board design issues involving signal integrity, the power supply, reference clocking, and trace design. {Lecture}
- **GTM Transceiver**
  Reviews GTM transceiver-specific design generation, simulation, implementation, and verification on real hardware. {Lecture, Labs targeting the VPK120 board}