AMD
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Designing FPGAs Using the Vivado Design Suite 4

FPGA-VDES4 (v1.0)

Course Specification

Course Description

Learn how to use the advanced aspects of the Vivado™ Design Suite.

The focus is on:

- Applying techniques to reduce delay and to improve clock skew and clock uncertainty
- Utilizing floorplanning techniques
- Employing advanced implementation options
- Utilizing AMD security features
- Identifying advanced FPGA configurations
- Debugging a design at the device startup phase
- Utilizing Tcl scripting when using the Vivado logic analyzer in a design

This is the final course in the *Designing FPGAs Using the Vivado Design Suite* series.

What's New for 2025.2

- All labs have been updated to the latest software versions

Level – FPGA 4

Course Details

- 2 days or 3 sessions 19

Course Part Number – FPGA-VDES4

Who Should Attend? – Engineers who seek advanced training in using AMD tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites

- Intermediate HDL knowledge (Verilog or VHDL)
- Sound digital design background
- *Designing FPGAs Using the Vivado Design Suite 1* (recommended)
- *Designing FPGAs Using the Vivado Design Suite 2* (recommended)
- *Designing FPGAs Using the Vivado Design Suite 3* (recommended)

Software Tools

- Vivado Design Suite 2025.2

Hardware

- Architecture: UltraScale™ FPGAs*
- Demo board: Zynq™ UltraScale+™ ZCU104 board*

* This course focuses on the UltraScale architectures. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Analyze a timing report to identify how to center the clock in the data eye
- Apply appropriate techniques to reduce logic and net delay and to improve clock skew and clock uncertainty
- Implement Intelligent Design Runs (IDR) to automate analysis and timing closure for complex designs
- Utilize floorplanning techniques to improve design performance
- Employ advanced implementation options, such as incremental compile flow, physical optimization techniques, and re-entrant mode as last mile strategies
- Utilize security features, bitstream encryption, and authentication using AES for design and IP security
- Identify advanced FPGA configurations, such as daisy chains and gangs, for configuring multiple FPGAs in a design
- Debug a design at the device startup phase to debug issues related to startup events, such as MMCM lock and design coming out of reset
- Utilize Tcl scripting when using the Vivado logic analyzer in a design

Course Outline

Day 1

UltraFast™ Design Methodology (UFDM)

- **UltraFast Design Methodology: Timing Closure**
  Introduces the UltraFast methodology guidelines on timing closure. {Lecture}

Vivado Tool Flow

- **Hierarchical Design**
  Provides an overview of the hierarchical design flows in the Vivado Design Suite. {Lecture}
- **Incremental Compile Flow**
  Demonstrates how to utilize the incremental compile flow when making last-minute RTL changes. {Lecture, Lab}
- **Vivado Design Suite ECO Flow**
  Illustrates using the ECO flow for making changes to a previously implemented design and applying the changes to the original design. {Lecture, Lab}

Vivado IP Catalog

- **Managing IP in Remote Locations**
  Covers storing IP and related files that are remote to the current working project directory. {Lecture, Lab}

Timing – Advanced

- **Timing Closure Using Physical Optimization Techniques**
  Describes physical optimization techniques for timing closure. {Lecture, Lab}
- **Reducing Logic Delay**
  Describes how to optimize regular fabric paths and paths with dedicated blocks and macro primitives. {Lecture}
- **Reducing Net Delay**
  Reviews different techniques to reduce congestion and net delay. {Lecture}
- **Improving Clock Skew**
  Describes how to apply various techniques to improve clock skew. {Lecture}
- **Improving Clock Uncertainty**
  Reviews various flows for improving clock uncertainty, including using parallel BUFGCE_DIV clock buffers, changing MMCM or PLL settings, and limiting synchronous clock domain crossing (CDC) paths. {Lecture, Lab}

Design Runs

- **Intelligent Design Runs (IDR)**
  Introduces Intelligent Design Runs (IDR), which are special types of implementation runs that use a complex flow to attempt to close timing. {Lecture, Lab}

Power

- **Power Management Techniques**
  Describes the techniques used for low power design. {Lecture}

Day 2

Floorplanning

- **Introduction to Floorplanning**
  Provides an introduction to floorplanning and how to use Pblocks while floorplanning. {Lecture}
- **Design Analysis and Floorplanning**
  Highlights the pre- and post-implementation design analysis features of the Vivado IDE. {Lecture, Lab}
- **Congestion**
  Identifies congestion and addresses congestion issues. {Lecture}

Configuration

- **Daisy Chains and Gangs in Configuration**
  Introduces advanced configuration schemes for multiple FPGAs. {Lecture}
- **Bitstream Security**
  Reviews AMD bitstream security features, such as readback disable, bitstream encryption, and authentication. {Lecture, Demo}

Debugging

- **Vivado Design Suite Debug Methodology**
  Covers debug core recommendations and how to employ the debug methodology for debugging a design using the Vivado logic analyzer. {Lecture}
- **Trigger and Debug at Device Startup**
  Shows how to debug the events around device startup. {Lecture, Demo}
- **Trigger Using the Trigger State Machine in the Vivado Logic Analyzer**
  Illustrates using trigger state machine code to trigger the ILA and capture data in the Vivado logic analyzer. {Lecture, Lab}

Vivado Store

- **Introduction to the Vivado Store**
  Introduces the Vivado Store. {Lecture, Demo}

Tcl Commands

- **Debugging a Design Using Tcl Commands**
  Reviews how to use Tcl scripting for VLA designs when adding probes and making connections to probes. {Lecture, Lab}
- **Using Procedures in Tcl Scripting**
  Discusses employing procedures in Tcl scripting. {Lecture}
- **Using Lists in Tcl Scripting**
  Covers how to employ lists in Tcl scripting. {Lecture}
- **Using Regular Expressions in Tcl Scripting**
  Highlights how to use regular expressions to find a pattern in a text file while scripting an action in the Vivado Design Suite. {Lecture, Lab}
- **Debugging and Error Handling in Tcl Scripts**
  Describes how to debug errors using Tcl scripts. {Lecture}

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