

Course Description

This course introduces the AMD Versal™ network on chip (NoC) to users familiar with other SoC architectures. Besides providing an overview of the major components in the Versal device, the course illustrates how the NoC can be configured to access DDR memory controllers and HBM memory controllers.

The emphasis of this course is on:

- Enumerating the major components comprising the NoC architecture in the Versal adaptive SoC
- Implementing a basic Versal NoC design using the Vivado™ IP integrator
- Accessing the Versal NoC using the modular NoC flow
- Configuring the DDR memory controller for accessing DDR memory
- Configuring and tuning the NoC for efficient data movement

What's New for 2025.2

- Added a new module on NoC DDR5 Memory Controller
- All labs have been updated to the latest software versions

Level – VER 2

Course Details

- 1 day ILT or 2 sessions/9

Course Part Number – VER-NOC

Who Should Attend? – Hardware developers and system architects—whether migrating from existing AMD SoC devices or starting out with the Versal devices

Prerequisites

- Any SoC or Versal adaptive SoC architecture course
- Familiarity with the Vivado Design Suite
- Familiarity with the Vitis™ Unified IDE

Software Tools

- Vivado Design Suite 2025.2
- Vitis Unified IDE 2025.2

Hardware

- Architecture: Versal adaptive SoCs

After completing this comprehensive training, you will have the necessary skills to:

- Identify the major network on chip components in the AMD Versal architecture
- Include the necessary components to access the NoC from the PL
- Access the Versal NoC resources using the IP integrator and/or modular NoC flow
- Design with the NoC and integrated DDR memory controller
- Configure connection QoS for efficient data movement

Course Outline

- **Architecture Overview for Existing Users**
Introduces to students who already have familiarity with AMD SoC architectures the new and updated features found in the Versal devices. Also provides an overview of the Versal portfolio. {Lecture}
- **NoC Introduction and Concepts**

Covers the reasons to use the network on chip, its basic elements, design entry flows, and common terminology. {Lecture, Lab}

- **NoC Architecture**

Provides a deep dive into the sub-blocks of the NoC and how they are used. Describes how the NoC is accessed from the programmable logic. {Lecture}

- **Design Tool Flow**

Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture}

- **Modular NoC Flow**

Introduces the modular NoC flow for accessing Versal NoC resources. Also discusses modular NoC flow-supported use cases. {Lecture, Lab}

- **NoC DDR4 Memory Controller**

The integration between the NoC pathways and the DDR4 memory controllers must be understood to have efficient data movement on and off chip. This discussion of the NoC's DDR4 memory controller blocks provides the background for properly selecting and configuring DDR4 memory and the memory controller for effective use. {Lecture, Lab}

- **NoC DDR5 Memory Controller**

The integration between the NoC pathways and the DDR5 memory controllers must be understood to have efficient data movement on and off chip. This discussion of the NoC's DDR5 memory controller blocks provides the background for properly selecting and configuring DDR5 memory and the memory controller for effective use. {Lecture, Lab}

- **NoC HBM Controller**

Describes the high-bandwidth memory (HBM) controller architecture and identifies the steps for HBM controller configuration. {Lecture}

- **NoC Performance Tuning**

Synthesizes everything about the NoC and its DDRMCs, illustrating how to fine tune the NoC for the best performance. {Lecture, Lab}