AMD
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Designing with the Spartan UltraScale+ FPGA: Architecture

FPGA-SU-ARCH (v1.0)

Course Specification

Course Description

Learn about the key features and architecture of the AMD Spartan™ UltraScale+™ FPGA, including its advanced I/O, high-speed transceivers, substantial built-in and external memory, PCIe® Gen4 connectivity, and modern security. Recognize how these features provide a versatile, cost-optimized, and power-efficient platform for diverse applications.

The emphasis of this course is on:

- Describing the key features and fundamental blocks of the Spartan UltraScale+ FPGA architecture
- Describing Spartan UltraScale+ clocking, including buffer types, clock management tiles, and routing for enhanced timing
- Describing the various on-chip memory resources available in the Spartan UltraScale+ architecture
- Utilizing the advanced I/O capabilities for various connectivity needs
- Identifying the high-speed transceivers for use in applications such as PCIe Gen4
- Explaining the configuration process for Spartan UltraScale+ devices
- Outlining the platform security framework and advanced security features
- Leveraging the Power Design Manager (PDM) tool for power estimation

What's New for 2025.2

- Added a new lab: MicroBlaze V Soft Processor Implementation
- All labs have been updated to the latest software versions

Level – FPGA 3

Course Details –

- 2 days ILT or 3 sessions/19
  Course Part Number – FPGA-SU-ARCH

Who Should Attend? – Anyone who would like to build a design for the Spartan UltraScale+ device

Prerequisites

- *Designing FPGAs Using the Vivado™ Design Suite 1* course
- *Designing with the UltraScale™ and UltraScale+ Architectures* course
- Familiarity with the Vivado Design Suite
- Intermediate VHDL or Verilog knowledge

Software Tools

- Vivado Design Suite 2025.2*
- Vitis Unified IDE 2025.2
- Power Design Manager tool 2025.2

Hardware

- Architecture: Spartan UltraScale+ FPGAs
- Demo board: Spartan UltraScale+ FPGA SCU35 Evaluation Kit

* Some tool features will be supported future releases.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the key features and fundamental blocks of the AMD Spartan UltraScale+ FPGA architecture
- Describe Spartan UltraScale+ clocking, including buffer types, clock management tiles, and routing for enhanced timing
- Describe the various on-chip memory resources available in the Spartan UltraScale+ architecture
- Utilize the advanced I/O capabilities for various connectivity needs
- Identify the high-speed transceivers for use in applications such as PCIe Gen4
- Explain the configuration process for Spartan UltraScale+ devices
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Course Outline

Day 1

- **Introduction to the AMD UltraScale+ Families**
  Describes how UltraScale+ architectural benefits and features deliver enhanced performance, efficiency, and flexibility across diverse product families. {Lecture}
- **Introduction to the AMD Spartan UltraScale+ Architecture**
  Discusses the key features and fundamental blocks of the Spartan UltraScale+ architecture. {Lecture, Lab}
- **Programmable Logic**
  Explores the Spartan UltraScale+ programmable logic architecture, including its core components, enhancements, and advanced routing capabilities. {Lecture}
- **Clocking Architecture, Buffers, CMTs, and Routing**
  Analyzes the Spartan UltraScale+ clocking architecture and resources, contrasting it with previous generations while exploring buffer types, clock management tiles (CMTs), and routing strategies for optimized timing. {Lecture, Lab}
- **Block RAM Memory Resources**
  Covers the Spartan UltraScale+ architecture block RAM configurations, features, and cascading modes. {Lecture}
- **FIFO Memory Resources**
  Outlines the capabilities of the built-in FIFO. {Lecture}
- **UltraRAM Resources**
  Explains the UltraRAM features and architecture. {Lecture}
- **I/O Resources Overview**
  Identifies high-speed I/O challenges and reviews the bank types available in Spartan UltraScale+ FPGAs while contrasting the architectural functionality of component and native modes. {Lecture, Lab}

Day 2

- **DSP Resources**
  Explores the architecture and functionality of the DSP48E2 slice in Spartan UltraScale+ FPGAs. {Lecture, Lab}
- **Transceivers**
  Describes the advancements and features of Spartan UltraScale+ transceivers compared to previous UltraScale architectures. {Lecture}
- **Transceivers Wizard**
  Reviews the functionality and benefits of the transceiver wizard. {Lecture}

- **PCI Express®**
  Discusses the architecture of the PCIe blocks in the Spartan UltraScale+ device and the differences between the different PCIe blocks. {Lecture}
- **Configuration**
  Provides an overview of the configuration process for Spartan UltraScale+ FPGAs. {Lecture}
- **Security Features**
  Describes the platform security framework offered by Spartan UltraScale+ devices. Also identifies the available advanced security features. {Lecture}
- **Power Design Manager**
  Explores the power estimation tools and how to utilize them for achieving better power efficiency using PDM. {Lecture, Lab}
- **Power Analysis and Optimization Using the AMD Vivado Design Suite**
  Describes how to estimate and analyze power consumption with the AMD Vivado Design Suite Power Report utility. {Lecture}

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