

Course Description

Learn how to build a more effective FPGA design.

The focus is on:

- Using synchronous design techniques
- Utilizing the Vivado™ IP integrator to create a sub-system
- Performing power analysis and optimization to improve the power efficiency of a design
- Reviewing and analyzing timing reports for a design

This course builds on the concepts from the *Designing FPGAs Using the Vivado Design Suite 1* course.

What's New for 2025.2

- All labs have been updated to the latest software versions

Level – FPGA 2

Course Details

- 2 days ILT or 3 sessions/19

Course Part Number – FPGA-VDES2

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to AMD FPGAs

Prerequisites

- Intermediate HDL knowledge (Verilog or VHDL)
- Digital design knowledge and experience (attendees should be electrical engineers)
- Experience with the basics of the Tcl language
- Designing FPGAs Using the Vivado Design Suite 1* (recommended)

Software Tools

- Vivado Design Suite 2025.2

Hardware

- Architecture: UltraScale™ FPGAs
- Demo board (optional): Zynq™ UltraScale+™ MPSoC ZCU104 board*

* This course focuses on the UltraScale architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify synchronous design techniques
- Build resets into your system for optimum reliability and design speed
- Create a Tcl script to create a project, add sources, and implement a design
- Describe and use the clock resources in a design
- Create and package your own IP and add to the Vivado IP catalog for reuse
- Use the Vivado IP integrator to create a block design
- Apply timing exception constraints in a design as part of the Baseline procedure to fine tune the design
- Perform power analysis and optimization
- Describe the HDL instantiation flow of the Vivado logic analyzer

Course Outline

Day 1

UltraFast™ Design Methodology

- UltraFast Design Methodology: Design Creation**
 Introduces the UltraFast methodology guidelines on design creation. {Lecture}
- Design Techniques**
 - Synchronous Design Techniques**
 Introduces the synchronous design techniques used in an FPGA design. {Lecture}
 - Resets**
 Investigates the impact of using asynchronous resets in a design. {Lecture, Lab}
 - Register Duplication**
 Covers the use of register duplication to reduce high fanout nets in a design. {Lecture}
 - Using Tcl Commands in the Vivado Design Suite Project Flow**
 Introduces basic Tcl commands and executing a Tcl script. {Lecture, Lab}
 - Scripting in Vivado Design Suite Non-Project Mode**
 Demonstrates how to write Tcl commands in the non-project batch flow for a design. {Lecture, Lab}

Clocking in the UltraScale Architecture

- Clock Structure and Layout in the UltraScale Architecture**
 Describes UltraScale clocking architecture and differences in the clocking architectures between 7 series and UltraScale FPGAs. {Lecture, Lab}
- Clock Buffers in the UltraScale Architecture**
 Reviews the different clock buffers and clock migration. {Lecture}
- Clock Management in the UltraScale Architecture**
 Highlights clock management resources. {Lecture}
- Clock Routing in the UltraScale Architecture**
 Describes clock routing, distribution, and the benefits of clock routing. {Lecture}

I/O in the UltraScale Architecture

- UltraScale Architecture I/O Resources: Overview**
 Provides an overview of the I/O resources and I/O banks available the UltraScale architecture. {Lecture}
- UltraScale Architecture I/O Resources: Component Mode**
 Describes component mode, SelectIO™ interface logic, SERDES technology, and programmable delay lines. {Lecture}
- UltraScale Architecture I/O Resources: Native Mode**
 Describes SelectIO interface logic, BITSlice technology, native mode clocking, and the High Speed SelectIO Wizard. {Lecture}

Day 2

IP Integrator

- Getting Started with Vivado IP Integrator**
 Introduces the Vivado IP integrator tool and its features. Also reviews creating and working with block designs. {Lecture, Demo, Lab}
- Designing IP Subsystems Using Vivado IP Integrator**
 Illustrates designing with processor-based subsystems and working with custom RTL code. Also explains how to create Vitis™ platforms using Vivado IP integrator. {Lecture}
- Block Design Containers in the Vivado IP Integrator**
 Describes the block design container (BDC) feature and shows how to create a BDC in the IP integrator. {Lecture}

- **Creating and Packaging Custom IP**
Covers creating your own IP and package and including it in the Vivado IP catalog. {Lecture, Lab}
- **Using an IP Container**
Illustrates how to use a core container file as a single file representation for an IP. {Lecture, Demo}

Timing – Intermediate

- **Report Clock Networks**
Demonstrates how to use the `report_clock_networks` command to view the primary and generated clocks in a design. {Lecture, Demo}
- **Timing Summary Report**
Reviews how to use the post-implementation timing summary report to sign off for timing closure. {Lecture, Demo}
- **Clock Group Constraints**
Describes applying clock group constraints for asynchronous clock domains. {Lecture, Demo}
- **Introduction to Timing Exceptions**
Introduces timing exception constraints and applying them to fine tune design timing. {Lecture, Demo, Lab}

Power

- **Power Analysis and Optimization Using the Vivado Design Suite**
Illustrates using report power commands to estimate power consumption. {Lecture, Lab}

Configuration

- **Configuration Process**
Reviews the FPGA configuration process, such as device power up and CRC checks. {Lecture}

Debugging

- **HDL Instantiation Debug Probing Flow**
Covers the HDL instantiation flow to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer. {Lecture, Lab}