

Course Description

This course provides a system-level understanding of AMD Versal™ adaptive SoC memory interfaces. Memory controller architecture, IP generation, simulation, and implementation are covered. Additional information on PCB design issues is also covered.

The focus is on:

- Constructing a system using Versal adaptive SoC external memory interfaces by:
 - Selecting the appropriate IP for an application
 - Configuring the memory controller IPs
 - Using the memory controllers in test benches and applications
 - Simulating and implementing the memory controller IPs
- Exploring traffic pattern generation
- Performance tuning for the hardened DDRMC
- Accessing the appropriate reference material for board design issues involving signal integrity, the power supply, reference clocking, and trace design

What's New for 2025.1

- New DDR5/LPDDR5 module with DDRMC5 content added
- New labs for DDRMC5 interface generation and simulation
- All labs have been updated to the latest software versions

Level – VER 3

Course Details

- 2 days ILT or 3 sessions/19

Course Part Number – VER-MEM

Who Should Attend?

- Hardware designers who want to create applications using external memory devices or modules
- System architects who want to leverage the key advantages of external memory interfaces

Prerequisites

- Knowledge of Verilog or VHDL
- Familiarity with logic design (state machines and synchronous design)
- Some experience with Vivado™ implementation
- Some experience with a simulation tool (preferably the Vivado simulator)
- Familiarity with DDR or LPDDR memories also helpful

Software Tools

- Vivado Design Suite 2025.1
- Vitis Unified IDE 2025.1

Hardware

- Architecture: All Versal adaptive SoC devices
- Evaluation board: Versal adaptive SoC VCK190 Evaluation Platform

After completing this comprehensive training, you will have the necessary skills to:

- Describe and utilize the building blocks of the hardened DDR memory controllers in AMD Versal devices

- Describe and utilize the ports and attributes of the hardened memory controllers
- Design, simulate, and implement designs using the hardened memory controllers
- Utilize DDR4/LPDDR4 debugging options
- Apply performance tuning options for linear and random traffic
- Identify memory interface board design requirements

Course Outline

Day 1

Versal Adaptive SoC: Architecture Overview for Existing Users

Introduces to students who already have familiarity with AMD SoC architectures the new and updated features found in the Versal devices. Also provides an overview of the Versal portfolio. {Lecture}

Network on Chip

Provides a deep dive into the sub-blocks of the NoC and how they are used. Describes how the NoC is accessed from the programmable logic. {Lecture}

Memory Solutions Overview

Identifies the external memory interfaces options for the Versal adaptive SoC and describes the main features of the hard and soft controllers. {Lecture}

DDR4 and LPDDR4 Memories

Discusses the DDR4 architectural and interface improvements and describes the LPDDR4 differences from DDR4. {Lecture}

DDR5 and LPDDR5 Memories

Reviews the DDR5/LPDDR5 architectural and interface improvements. {Lecture}

Hardened DDR Memory Controllers

Describes the architecture and functionality of the hardened DDR memory controllers and the PHY block. {Lecture}

Configuring the Hardened DDR Memory Controllers

Covers how to perform hardened DDR memory controller configuration and provides background information for selecting optimal parameters. {Lecture, Labs}

Simulating the Hardened DDR Memory Controllers

Illustrates how to perform hardened DDR memory controller simulation and describes the creation of test benches. {Lecture, Labs}

Day 2

Implementing the Hardened DDR Memory Controllers

Demonstrates how to perform DDR memory controller implementation with a brief discussion of the pin planning process. {Lecture, Lab}

DDRMC Performance Tuning

Discusses quality of service (QoS) and bandwidth aspects and provides a detailed description of performance tuning options. {Lecture, Lab}

Debugging the Memory Interfaces

Outlines various options to debug memory interfaces. {Lecture, Lab}

- **DDR4 Soft Controller**
Reviews the basic architecture and functionality of the DDR4 soft controller and describes the traditional design flow for all soft controllers. {Lecture}
- **Memory Interfaces PCB Design**
Describes board design issues involving signal integrity, the power supply, reference clocking, and trace design. {Lecture}

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