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Migrating from UltraScale+ Devices to Versal Adaptive SoCs

VER MGRT (v1.0)

Course Specification

Course Description

This course illustrates the different approaches for efficiently migrating existing designs to the AMD Versal™ adaptive SoC from AMD UltraScale+™ devices. The course also covers system design planning and partitioning methodologies as well as design migration considerations for different system design types.

The emphasis of this course is on:

- Identifying and comparing various functional blocks in the Versal adaptive SoC to those in previous-generation UltraScale+ devices
- Reviewing the approaches for migrating existing designs to the Versal adaptive SoC
- Describing the development platforms for all developers
- Enabling top-level RTL flows for Versal devices
- Identifying design migration considerations for PL-only designs and Zynq™ UltraScale+ MPSoC designs
- Specifying the recommended methodology for planning a system design migration based on the system design type
- Discussing AI Engine system partitioning planning
- Migrating Zynq UltraScale+ MPSoC-based system-level designs to the Versal adaptive SoC
- Detailing Versal device hardware debug features

What's New for 2025.1

- Architecture Overview for Existing Users module: Added Versal AI Edge Series Gen 2 and Prime Series Gen 2 details
- System Design Migration Approach module: Updated Versal PCIe® solutions and added enhanced embedded system security for Versal AI Edge Series Gen 2 and Prime Series Gen 2 details
- Processing System Comparison module: Added Versal AI Edge Series Gen 2 and Prime Series Gen 2 processing system information
- AI Engine Architecture Overview and Programming module: Introduced the AIE-ML v2 architecture
- All labs have been updated to the latest software versions

Level – VER 2

Course Details

- 1 day ILT or 2 sessions/9

Course Part Number – VER MGRT

Who Should Attend? – Software and hardware developers, system architects, and anyone who needs to migrate their designs to Versal devices

Prerequisites

- Familiarity with designing UltraScale+ FPGAs and adaptive SoCs
- Familiarity with the AMD Vivado™ and Vitis™ tools

Software Tools

- Vivado Design Suite 2025.1
- Vitis Unified IDE 2025.1

Hardware

- Architecture: Versal adaptive SoC

After completing this comprehensive training, you will have the necessary skills to:

- Identify the different functional blocks in the AMD Versal adaptive SoC
- Utilize high-level system migration steps for efficient migration to the Versal adaptive SoC
- Describe the different tool flows for the Versal adaptive SoC
- Implement a basic Versal NoC design
- Utilize top-level RTL flows such as the modular NoC flow and GT subsystem flow for Versal devices
- Apply design migration guidelines for PL-only and PS+PL designs
- Follow the system design planning methodology
- Describe the AI Engine architecture and programming model as well as follow the AIE system partitioning methodology
- Migrate AMD Zynq UltraScale+ MPSoC system-level designs to the Versal adaptive SoC
- Describe the different debugging options available for the Versal adaptive SoC

Course Outline

- **Architecture Overview for Existing Users**
  Introduces to students who already have familiarity with AMD SoC architectures the new and updated features found in the Versal devices. Also provides an overview of the Versal portfolio. {Lecture}
- **System Design Migration Approach**
  Describes important system design migration considerations and the high-level system steps for efficient migration to the Versal adaptive SoC. Also compares various functional blocks in the Versal adaptive SoC to those in previous-generation devices. {Lecture}
- **Design Tool Flow**
  Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture}
- **NoC Introduction and Concepts**
  Covers the reasons to use the network on chip, its basic elements, design entry flows, and common terminology. {Lecture, Lab}
- **Enabling Top-level RTL Flows**
  Discusses two RTL-centric flows: One for accessing the NoC from RTL, known as the modular NoC flow, and another for the gigabit transceivers with the GT Wizard Subsystem flow. {Lecture, Labs}
- **Programmable Logic Design Migration Considerations**
  Describes Versal adaptive SoC architectural enhancements as well as key programmable logic design migration considerations and best practices. Also covers the advantages of the Advanced Flow for Versal devices. {Lecture, Labs}
- **Processing System Comparison**
  Describes Versal adaptive SoC processing system architectural differences. It covers the differences in the boot sequence between Versal and Zynq UltraScale+ devices. Also introduces the segmented configuration feature for Versal devices. {Lecture}
- **System Design Planning Methodology**
  Describes system design planning, power, and thermal guidelines. Also reviews system debug, verification, and validation planning. {Lecture}
- **AI Engine Architecture Overview and Programming**
  Discusses the Versal AI Engine architecture and explains the programming model for AI Engines with kernels and graph. {Lecture}

- **AI Engine System Partitioning**
  Describes the AI Engine system partitioning and planning methodology and mapping system requirements. {Lecture, Lab}
- **System-level Design Migration**
  Demonstrates how to migrate a Zynq UltraScale+ MPSoC system-level design to the Versal adaptive SoC. Also shows how to implement the same system design on the Versal AI Engine. {Lab}
- **Debug Overview**
  Describes the tools and techniques available to debug PL and hard blocks in Versal devices. Also covers ChipScoPy APIs, which provide a Python™ interface to program and debug Versal devices. {Lecture}