

Course Description

This course provides software developers options and techniques for selecting and implementing various types of operating systems and hypervisors on AMD Zynq™ UltraScale+™ and Versal™ devices.

The emphasis is on:

- Exploring the capabilities of the application processing unit (APU) and real-time processing unit (RPU) relative to performance improvement and OS implementation
- Reviewing the catalog of OS implementation options, including Arm® TrustZone technology, hypervisors, and various Linux® implementations
- Applying various power management techniques for Zynq UltraScale+ and Versal devices

What's New for 2024.1

- All labs have been updated according to the latest tool release.
- The lab on PMU: System Power Management has been added.

Level – Embedded Software 3

Course Details

- 3 days ILT /29

Course Part Number – SOC-OS-HYPER

Who Should Attend? – Software developers interested in understanding popular OS and hypervisor options and other high-level system design issues.

Prerequisites

- General understanding of C coding
- Familiarity with issues related to complex embedded systems

Software Tools

- Vivado™ Design Suite 2024.1
- Vitis™ Unified IDE 2024.1
- Hardware emulation environment:
 - VirtualBox/CloudShare
 - QEMU
 - Ubuntu® desktop
 - PetaLinux

Hardware

- Zynq UltraScale+ MPSoC ZCU104 board*
- Versal adaptive SoC VCK190 board

* This course focuses on the Zynq UltraScale+ and Versal architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab environment or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Leverage the innate capabilities of the application processing unit (APU) and real-time processing unit (RPU)
- Investigate Arm TrustZone technology
- Explore the concept of hypervisors and implement a Xen hypervisor example
- Implement Linux solutions, including asymmetric multiprocessing (AMP) and symmetric multiprocessing (SMP) configurations
- Deploy FreeRTOS in the RPU
- Effectively use power management strategies

Course Outline

Day 1

Application Processing Unit

Introduction to the members of the APU, specifically the Arm® Cortex®-A53 processor and how the cluster is configured and managed. {Lectures, Lab}

Real-Time Processing Unit

Focuses on the real-time processing module (RPU) in the PS, which is comprised of a pair of Arm Cortex processors and supporting elements. {Lectures, Demo, Lab}

Arm TrustZone Technology

Illustrates the use of Arm TrustZone technology. {Lectures}

QEMU

Introduction to the Quick Emulator, which is the tool used to run software for a device when hardware is not available. {Lectures, Demo, Lab}

HW-SW Virtualization

Covers the hardware and software elements of virtualization. {Lecture}

Day 2

Multiprocessor Software Architecture

Focuses on how multiple processors can communicate with each other using both software and hardware techniques. {Lecture}

Xen Hypervisor

Discusses generic hypervisors and reviews some of the details of implementing a hypervisor using Xen. {Lectures, Demo, Lab}

OpenAMP

Discusses how the OpenAMP framework can be used to construct systems containing both Linux and Standalone applications within the APU. {Lectures, Lab}

Linux

Describes how to configure Linux to manage multiple processors. {Lectures, Demo}

Driving the PetaLinux Tool

Introduces the basic concepts required to build an application using the PetaLinux tool. {Lecture, Lab}

Yocto

Compares and contrasts the kernel building methods between a "pure" Yocto build and the PetaLinux build (which uses Yocto "under the hood"). {Lectures, Lab}

Open-Source Library (Linux)

Introduction to open-source Linux and how the PetaLinux tools reduce effort and risk. {Lectures, Demo}

Day 3

FreeRTOS

Overview of FreeRTOS with examples of how it can be used. {Lectures, Demo, Lab}

Software Stack

Introduction to what a software stack is and a number of commonly used stacks. {Lectures, Demo}

Power Management

Introduction to the concepts of power requirements in embedded systems and the Zynq UltraScale+ MPSoC. {Lectures, Lab}