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Migrating from UltraScale+ Devices to Versal Adaptive SoCs

ACAP MGRT (v1.0)

Course Specification

Course Description

This course illustrates the different approaches for efficiently migrating existing designs to the AMD Versal™ adaptive SoC from AMD UltraScale+™ devices. The course also covers system design planning and partitioning methodologies as well as design migration considerations for different system design types.

The emphasis of this course is on:

- Identifying and comparing various functional blocks in the Versal adaptive SoC to those in previous-generation UltraScale+ devices
- Describing the development platforms for all developers
- Reviewing the approaches for migrating existing designs to the Versal adaptive SoC
- Specifying the recommended methodology for planning a system design migration based on the system design type
- Discussing AI Engine system partitioning planning
- Identifying design migration considerations for PL-only designs and Zynq™ UltraScale+ MPSoC designs
- Migrating Zynq UltraScale+ MPSoC-based system-level designs to the Versal adaptive SoC
- Detailing Versal device hardware debug features

Level – ACAP 2

Course Details

- 1 day ILT

Course Part Number – ACAP MGRT

Who Should Attend? – Software and hardware developers, system architects, and anyone who needs to migrate their designs to Versal devices

Prerequisites

- Familiarity with designing UltraScale+ FPGAs and adaptive SoCs
- Familiarity with the AMD Vivado™ and Vitis™ tools

Software Tools

- Vivado Design Suite 2024.1
- Vitis Unified IDE 2024.1

Hardware

- Architecture: Versal adaptive SoC

After completing this comprehensive training, you will have the necessary skills to:

- Identify the different functional blocks in the AMD Versal adaptive SoC
- Describe the different tool flows for the Versal adaptive SoC
- Utilize high-level system migration steps for efficient migration to the Versal adaptive SoC
- Follow the system design planning methodology
- Apply design migration guidelines for PL-only and PS+PL designs
- Describe the AI Engine architecture and programming model as well as follow the AIE system partitioning methodology
- Migrate AMD Zynq UltraScale+ MPSoC system-level designs to the Versal adaptive SoC
- Describe the different debugging options available for the Versal adaptive SoC

Course Outline

- **Architecture Overview for Existing UltraScale+ Users**
  Introduces to users who are already familiar with the UltraScale+ architectures the new and updated features found in the Versal devices. Also provides an overview of the Versal portfolio. {Lecture}
- **Design Tool Flow**
  Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly. {Lecture, Lab}
- **System Design Migration Approach**
  Describes important system design migration considerations and the high-level system steps for efficient migration to the Versal adaptive SoC. Also compares various functional blocks in the Versal adaptive SoC to those in previous-generation devices. {Lecture}
- **System Design Planning Methodology**
  Describes system design planning, power, and thermal guidelines. Also reviews system debug, verification, and validation planning. {Lecture}
- **Programmable Logic Design Migration Considerations**
  Describes Versal adaptive SoC architectural enhancements as well as key programmable logic design migration considerations and best practices. {Lecture, Labs}
- **Processing System Comparison**
  Describes Versal adaptive SoC processing system architectural differences. Also covers the differences in the boot sequence between Versal and Zynq UltraScale+ devices. {Lecture}
- **AI Engine Architecture Overview and Programming**
  Discusses the Versal AI Engine architecture and explains the programming model for AI Engines with kernels and graph. {Lecture}
- **AI Engine System Partitioning**
  Describes the AI Engine system partitioning and planning methodology and mapping system requirements. {Lecture, Lab}
- **System Migration**
  Demonstrates how to migrate a Zynq UltraScale+ MPSoC system-level design to the Versal adaptive SoC. Also shows how to implement the same system design on the Versal AI Engine. {Lab}
- **Debug Overview**
  Describes the tools and techniques available to debug PL and hard blocks in Versal devices. Also covers ChipScoPy APIs, which provide a Python™ interface to program and debug Versal devices. {Lecture}

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