

FPGA-VDES1 (v1.0)

Course Specification

Course Description

This course offers introductory training on the AMD Vivado™ Design Suite and demonstrates the FPGA design flow for those uninitiated to FPGA design.

The course provides experience with:

- Creating a Vivado Design Suite project with source files
- Simulating a design
- Performing pin assignments
- Applying basic timing constraints
- Synthesizing and implementing
- Debugging a design
- Generating and downloading a bitstream onto a demo board

What's New for 2024.1

- Synthesis and Implementation and Bitstream Generation module: Added information about the Dataflow Viewer feature
- All labs have been updated to the latest software versions

Level – FPGA 1

Course Details

- 2 days ILT/19

Course Part Number – FPGA-VDES1

Who Should Attend? – Digital designers new to FPGA design who need to learn the FPGA design cycle and the major aspects of the Vivado Design Suite

Prerequisites

- Basic knowledge of the VHDL or Verilog language
- Digital design knowledge

Software Tools

- Vivado Design Suite 2024.1

Hardware

- Architecture: UltraScale™ FPGAs
- Demo board: Zynq™ UltraScale+™ MPSoC ZCU104 board*

* This course focuses on the UltraScale architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the New Project Wizard to create a new Vivado IDE project
- Describe the supported design flows of the Vivado IDE
- Generate a DRC report to detect and fix design issues early in the flow
- Use the Vivado IDE I/O Planning layout to perform pin assignments
- Perform clocking and static timing analysis (STA)
- Synthesize and implement an HDL design
- Apply clock and I/O timing constraints and perform timing analysis
- Use the Xilinx Power Estimator (XPE) tool to estimate power
- Use the Schematic and Hierarchy viewers to analyze and cross-probe a design
- Use the Vivado logic analyzer and debug cores to debug a design

Course Outline

Day 1

Device Architectures

- **Introduction to FPGAs**
Provides an overview of FPGA architecture and describes the advantages, applications, and major building blocks of FPGAs. {Lecture}
- **AMD FPGA and Adaptive SoC Portfolio**
Introduces 7 series and UltraScale FPGAs, stacked silicon interconnect-based 3D IC devices, Zynq 7000 SoCs, Zynq UltraScale+ MPSoCs, and Versal™ adaptive SoCs. {Lecture}

Vivado IDE Overview

- **Introduction to the Vivado Design Suite**
Describes various design flows and the role of the Vivado IDE in the flows. {Lecture}
- **Introduction to the Tcl Environment**
Introduces Tcl (tool command language). {Lecture}
- **Vivado Design Suite Project-Based Mode**
Introduces project-based mode in the Vivado Design Suite, including creating a project, adding files to a project, exploring the Vivado IDE, and simulating a design. {Lecture, Lab}
- **Vivado Design Suite Non-Project Based Mode**
Describes the design flow using non-project batch mode, including using design analysis commands and how constraints are managed in non-project mode. {Lecture}

UltraFast™ Design Methodology

- **UltraFast Design Methodology: Board and Device Planning**
Introduces the methodology guidelines on board and device planning. {Lecture}

Vivado Tool Flow

- **RTL Development**
Covers RTL and the RTL design flow, recommended coding guidelines, using control signals, and recommendations on resets. {Lecture}
- **Behavioral Simulation**
Describes the process of behavioral simulation and the simulation options available in the Vivado IDE. {Lecture}
- **Vivado IP Flow**
Demonstrates how to customize IP, instantiate IP, and verify the hierarchy of your design IP. {Lecture, Demo, Lab}
- **Vivado Synthesis and Implementation and Bitstream Generation**
Reviews creating timing constraints according to the design scenario, synthesizing and implementing the design, and, optionally, generating and downloading a bitstream to a demo board. {Lecture, Lab}

Design Analysis

- **Basic Design Analysis in the Vivado IDE**
Outlines the various design analysis features in the Vivado Design Suite. {Demo, Lab}
- **Vivado Design Rule Checks**
Illustrates how to run a DRC report on the elaborated design to detect design issues early in the flow. Fix the DRC violations. {Lab}
- **Introduction to Vivado Reports**
Demonstrates generating and using Vivado timing reports to analyze failed timing paths. {Lecture, Demo}

Day 2

Timing – Basics

- **Introduction to Clock Constraints**
Shows how to apply clock constraints and perform timing analysis. {Lecture, Demo, Lab}
- **Generated Clocks**
Demonstrates using the report clock networks report to determine if there are any generated clocks in a design. {Lecture, Demo}
- **I/O Constraints and Virtual Clocks**
Covers applying I/O constraints and performing timing analysis. {Lecture, Lab}
- **Timing Constraints Wizard**
Reviews how use the Timing Constraints Wizard to apply missing timing constraints in a design. {Lecture, Lab}
- **Static Timing Analysis (STA)**
Describes the clock and its attributes, basics of clock gating, and static timing analysis (STA). {Lecture}
- **Setup and Hold Violation Analysis**
Covers what setup and hold slack are and describes how to perform input/output setup and hold analysis. {Lecture}

Pin Planning

- **Vivado Design Suite I/O Pin Planning**
Describes the I/O Pin Planning layout for performing pin assignments in a design. {Lecture, Lab}

Power

- **Power Estimation Using XPE**
Illustrates estimating the amount of resources and default activity rates for a design and evaluating the estimated power calculated by XPE. {Lecture, Lab}
- **Understanding Design Power**
Describes the importance of power closure and device selection for better time to market. {Lecture}
- **Versal Adaptive SoC Power Design Manager**
Discusses using the Power Design Manager tool, including import and export functions. {Lecture}

Configuration

- **Introduction to FPGA Configuration**
Describes how FPGAs can be configured. {Lecture}

Debugging

- **Introduction to the Vivado Logic Analyzer**
Provides an overview of the Vivado logic analyzer for debugging a design. {Lecture, Demo}
- **Introduction to Triggering**
Introduces the trigger capabilities of the Vivado logic analyzer. {Lecture}
- **Debug Cores**
Describes how the debug hub core is used to connect debug cores in a design. {Lecture}