AMD
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Designing with the Versal Adaptive SoC: Network on Chip

ACAP-NOC (v1.0)

Course Specification

Course Description

This course introduces the AMD Versal™ network on chip (NoC) to users familiar with other SoC architectures. Besides providing an overview of the major components in the Versal device, the course illustrates how the NoC is used to efficiently move data within the device.

The emphasis of this course is on:

- Enumerating the major components comprising the NoC architecture in the Versal adaptive SoC
- Implementing a basic design using the NoC
- Configuring the NoC for efficient data movement

What's New for 2024.1

- All labs have been updated to the latest software versions

Level – ACAP 2

Course Details

- 1 day ILT/9

Course Part Number – ACAP-NOC

Who Should Attend? – Hardware developers and system architects—whether migrating from existing AMD SoC devices or starting out with the Versal devices

Prerequisites

- Any SoC or Versal adaptive SoC architecture course
- Familiarity with the Vivado™ Design Suite
- Familiarity with the Vitis™ Unified IDE

Software Tools

- Vivado Design Suite 2024.1
- Vitis Unified IDE 2024.1

Hardware

- Architecture: Versal adaptive SoCs

After completing this comprehensive training, you will have the necessary skills to:

- Identify the major network on chip components in the AMD Versal architecture
- Include the necessary components to access the NoC from the PL
- Configure connection QoS for efficient data movement

Course Outline

- **Architecture Overview for Existing Users**

  Introduces to students who already have familiarity with AMD SoC architectures the new and updated features found in the Versal devices. {Lecture}
- **Versal Adaptive SoCs Compared to Zynq UltraScale+ Devices**

  The Versal adaptive SoC has a number of similarities to the Zynq™ UltraScale+™ MPSoC devices. Understanding what is the same, what is different, and what is brand new helps put this powerful new part into context. {Lecture}
- **NoC Introduction and Concepts**

  Reviews the basic vocabulary and high-level operations of the NoC. {Lecture, Lab}
- **NoC Architecture**

  Provides the first deep dive into the sub-blocks of the NoC and how they are used. Describes how the NoC is accessed from the programmable logic. {Lecture}
- **Design Tool Flow**

  Designers come to the Versal devices with different goals. This module explores how traditional FPGA designers, embedded developers, and accelerated system designers would leverage the most appropriate tools. {Lecture}
- **NoC DDR Memory Controller**

  The integration between the NoC pathways and the DDR memory controllers must be understood to have efficient data movement on and off chip. This discussion of the NoC's DDR memory controller blocks provides the background for properly selecting and configuring DDR memory and the memory controller for effective use. {Lecture, Lab}
- **NoC Performance Tuning**

  Synthesizes everything about the NoC and its DDRMCs, illustrating how to fine tune the NoC for the best performance. {Lecture, Lab}
- **System Design Migration**

  Describes how different users will leverage tools and processes to migrate their designs to the Versal devices. {Lecture}