



Designing with the Zynq UltraScale+ RFSoc

CONN-RFSOC (v1.0)

Course Specification

Course Description

This course provides an overview of the hard block capabilities for the Zynq® UltraScale+™ RFSoc family with a special emphasis on the RF Data Converter and Soft-Decision FEC blocks.

The focus is on:

- Describing the RFSoc family in general
- Identifying applications for the RF Data Converter and SD-FEC blocks
- Configuring, simulating, and implementing the blocks
- Verifying the RF Data Converter on real hardware
- Reviewing power estimation to help identify the power demands of the RFSoc device in various operating modes
- Identifying proper layout and PCB considerations since the Zynq UltraScale+ RFSoc is both a high-speed and an analog and digital device

What's New for 2022.1

- *General*
 - Update to Gen3 devices
 - DFE devices added
 - Labs updated to 2022.1 software
- *Frequency Planning Modules*
 - New Frequency Planner tool
 - Practice targets the new tool
- *Data Converter Practice*
 - Updated to 2022.1 software
 - RF data converter design example supported in ILT version only (requires 2020.1 software)

Level – Connectivity 3

Course Details

- 4 days – 6 hours each (3-day class)
 - 37 lectures
 - 8 labs
 - 3 demos

Price –

Course Part Number – CONN-RFSOC

Who Should Attend? – **System Architects & Hardware Designers** interested in understanding the architecture and capabilities of the Zynq UltraScale+ RFSoc data converter and SD-FEC hard blocks.

Prerequisites

- Suggested: Understanding of the Zynq UltraScale+ MPSoC architecture
- Basic familiarity with data converter terms and principles
- Basic familiarity with forward error correction terms and principles

Software Tools

- Vivado® Design Suite 2022.1
- Vitis unified software platform 2022.1

Hardware

- Host computer for running the above software
- Zynq UltraScale+ RFSoc ZCU111 board*

* This course focuses on the Zynq UltraScale+ RFSoc architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe in general the new Zynq UltraScale+ RFSoc family
- Identify typical applications for the RF data converters
- Describe the architecture and functionality of the RF-ADC
- Utilize the RF-ADC via configuration, simulation, and implementation
- Describe the architecture and functionality of the RF-DAC
- Utilize the RF-DAC via configuration, simulation, and implementation
- Identify the requirements and options for data converter PCB designs
- Describe the architecture and functionality of the Soft-Decision FEC hard IP
- Utilize the Soft-Decision FEC via configuration and simulation

Course Outline

- **Zynq UltraScale+ RFSoc Overview**
Overview of the Zynq UltraScale+ RFSoc architecture, including brief introductions to RF, RF data converter solutions, SD-FEC solutions, driver support, and tool support. {Lectures, Demo}
- **RF-ADC Hardware**
Covers the basics of RF-ADCs. Reviews RF-ADC architecture, functionality, interfaces, configuration, and driver support. {Lectures, Demo, Lab}
- **RF-DAC Hardware**
Covers the basics of RF-DACs. Reviews RF-DAC architecture, functionality, interfaces, configuration, and driver support. {Lectures, Demo, Lab}
- **RFSoc Hardware**
Provides an overview of the ZCU111 board and describes board setup. {Lectures}
- **Data Converter Design**
Describes common features, the design flow, utilizing the example design by simulation and implementation, and verifying RF data converter functionality on real hardware. Includes practice of using a software driver to modify RF data converter parameters. {Lectures, Labs}
- **Data Converter Practice**
Provides practical RF data converter experience using the ZCU111 board evaluation tool and RF analyzer tool. Demonstrates a PYNQ-based application to validate QPSK streams. Describes RF data converter frequency planning. Utilizes an RF data converter design example. {Lectures, Practices}
- **PCB Design for RFSoc Devices**
Describes power requirements, performing power estimation, and utilizing the power design. Analog signal requirements, PCB materials and layer stackup options, and analog trace design are also covered. {Lectures, Demo, Lab}
- **Soft-Decision FEC Hardware**
Covers the basics of forward error correction. Reviews SD-FEC architecture, functionality, interfaces, configuration, and driver support. {Lectures, Demo, Labs}