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Zynq UltraScale+ MPSoC for the Hardware Designer

EMBD-ZUPHW (v1.0)

Course Specification

Course Description

This course provides hardware designers with an overview of the capabilities and support for the AMD Zynq™ UltraScale+™ MPSoC family from a hardware architectural perspective.

The emphasis is on:

- Identifying the key elements of the application processing unit (APU) and real-time processing unit (RPU)
- Reviewing the various power domains and their control structure
- Illustrating the processing system (PS) and programmable logic (PL) connectivity
- Utilizing QEMU to emulate hardware behavior

What's New for 2023.2

- All labs have been updated to the latest software versions
- All labs and demos have been migrated to the new Vitis Unified IDE.

Level – Embedded Hardware 3

Course Details

- 2 days ILT /19

Course Part Number – EMBD-ZUPHW

Who Should Attend? – Hardware designers interested in understanding the architecture and capabilities of the Zynq UltraScale+ MPSoC device.

Prerequisites

- Suggested: Understanding of the Zynq 7000 architecture
- Basic familiarity with embedded software development using C (to support testing of specific architectural elements)

Software Tools

- Vivado™ Design Suite 2023.2
- Vitis™ Unified IDE 2023.2
- Hardware emulation environment:
  - VirtualBox
  - QEMU
  - Ubuntu desktop
  - PetaLinux

Hardware

- Zynq UltraScale+ MPSoC ZCU104 board*
- Zynq 7000 SoC ZC702 board*
- Versal™ adaptive SoC VCK190 board*

* This course focuses on the Zynq UltraScale+ MPSoC, Zynq 7000 SoC, and Versal adaptive SoC architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab environment or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Enumerate the key elements of the application processing unit (APU) and real-time processing unit (RPU)
- List the various power domains and how they are controlled
- Describe the connectivity between the processing system (PS) and programmable logic (PL)
- Utilize QEMU to emulate hardware behavior

Course Outline

Day 1

- **Application Processing Unit**
  Introduction to the members of the APU, specifically the Arm® Cortex®-A53 processor and how the cluster is configured and managed. {Lectures, Lab}
- **Real-Time Processing Unit**
  Focuses on the real-time processing module (RPU) in the PS, which is comprised of a pair of Cortex processors and supporting elements. {Lectures, Demo, Lab}
- **QEMU**
  Introduction to the Quick Emulator, which is the tool used to run software for the Zynq UltraScale+ MPSoC device when hardware is not available. {Lectures, Demo, Labs}
- **Booting**
  How to implement the embedded system, including the boot process and boot image creation. {Lectures, Lab}
- **First Stage Boot Loader**
  Demonstrates the process of developing, customizing, and debugging this mandatory piece of code. {Lecture, Demo}

Day 2

- **Video**
  Introduction to video, video codecs, and the video codec unit available in the Zynq UltraScale MPSoC. {Lectures}
- **System Protection**
  Covers all the hardware elements that support the separation of software domains. {Lectures}
- **Clocks and Resets**
  Overview of clocking and reset, focusing more on capabilities than specific implementations. {Lectures, Demos}
- **AXI**
  Understanding how the PS and PL connect enables designers to create more efficient systems. {Lectures, Demo, Lab}
- **Power Management and the PMU**
  Overview of the PMU and the power-saving features of the device. {Lectures}
- **Debugging Using Cross-Triggering**
  Illustrates how HW-SW cross-triggering techniques can uncover issues. {Lecture, Lab}

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