AMD
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Designing with the Versal Adaptive SoC: Memory Interfaces

ACAP-MEM (v1.0)

Course Specification

Course Description

This course provides a system-level understanding of AMD Versal™ adaptive SoC memory interfaces. Memory controller architecture, IP generation, simulation, and implementation are covered. Additional information on PCB design issues is also covered.

The focus is on:

- Constructing a system using Versal adaptive SoC external memory interfaces by:
  - Selecting the appropriate IP for an application
  - Configuring the memory controller IPs
  - Using the memory controllers in test benches and applications
  - Simulating and implementing the memory controller IPs
- Exploring traffic pattern generation
- Performance tuning for the hardened DDRMC
- Accessing the appropriate reference material for board design issues involving signal integrity, the power supply, reference clocking, and trace design

What's New for 2023.2

- All labs have been updated to the latest software versions
- Debugging lab now uses the Vitis™ Unified IDE

Level – ACAP 3

Course Details

- 2 days ILT /19

Course Part Number – ACAP-MEM

Who Should Attend?

- Hardware designers who want to create applications using external memory devices or modules
- System architects who want to leverage the key advantages of external memory interfaces

Prerequisites

- Knowledge of Verilog or VHDL
- Familiarity with logic design (state machines and synchronous design)
- Some experience with Vivado™ implementation
- Some experience with a simulation tool (preferably the Vivado simulator)
- Familiarity with DDR4 or LPDDR memories also helpful

Software Tools

- Vivado Design Suite 2023.2
- Vitis Unified IDE 2023.2

Hardware

- Architecture: All Versal adaptive SoC devices
- Evaluation board: Versal adaptive SoC VCK190 Evaluation Platform

After completing this comprehensive training, you will have the necessary skills to:

- Describe and utilize the building blocks of the DDRMC in AMD Versal devices
- Describe and utilize the ports and attributes of the DDRMC
- Design, simulate, and implement designs using the hardened memory controller
- Utilize DDR4/LPDDR4 debugging options
- Apply performance tuning options for linear and random traffic
- Describe memory interface board design requirements

Course Outline

Day 1

- **Versal Adaptive SoC: Architecture Overview for Existing Users**
  Provides an introduction to the Versal architecture. {Lecture}
- **Memory Solutions Overview**
  Identifies the external memory interfaces options for the Versal adaptive SoC and describes the main features of the hard and soft controllers. {Lecture}
- **DDR4 and LPDDR4 Memories**
  Discusses the DDR4 architectural and interface improvements and describes the LPDDR4 differences from DDR4. {Lecture}
- **DDRMC Hardened Memory Controller**
  Describes the architecture and functionality of the DDRMC and the PHY block. {Lecture}
- **Configuring the DDRMC Hard Controller**
  Covers how to perform DDRMC configuration and provides background information for selecting optimal parameters. {Lecture, Lab}
- **Simulating the DDRMC Hard Controller**
  Illustrates how to perform DDRMC simulation and describes the creation of test benches. {Lecture, Lab}

Day 2

- **Implementing the DDRMC Hard Controller**
  Demonstrates how to perform DDRMC implementation with a brief discussion of the pin planning process. {Lecture, Lab}
- **DDRMC Performance Tuning**
  Discusses quality of service (QoS) and bandwidth aspects and provides a detailed description of performance tuning options. {Lecture, Lab}
- **Debugging Memory Interfaces**
  Outlines various options to debug memory interfaces. {Lecture, Lab}
- **DDR4 Soft Controller**
  Reviews the basic architecture and functionality of the DDR4 soft controller and describes the traditional design flow for all soft controllers. {Lecture}
- **Memory Interfaces PCB Design**
  Describes board design issues involving signal integrity, the power supply, reference clocking, and trace design. {Lecture}