Vivado FPGA Design Essentials

FPGA-VDES-1-2-UFDM-COMBINED (v1.1)

Course Description

This course covers all essential Xilinx FPGA design concepts. It affords you a solid foundation for leveraging Xilinx tools and technology. We cover every aspect of FPGA design, from architectural considerations, to detailed timing constraints and static-timing-analysis (STA), to individual designer productivity. The comprehensive range of topics derives from combining elements of both the "FPGA Design with Vivado DS" – Level 1 & Level 2 courses, along with the "Ultra-Fast Design Methodology" course. This results in a uniquely broad range of coverage and skillsets packaged in a cost-effective time frame. That maximizes your training budget ROI. Each session is organized to reinforce learning and retention. Beyond the raw data, our certified instructors provide over-arching context and FPGA design insights.

The emphasis of this course is on:

- Getting started with Vivado DS
- Effective and compete timing constraints
- Key reports for analysis and debug
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Level – FPGA 1 & 2

Course Details

- 3 day classroom training / onsite
- 24 hours online (4 sessions, 6 hr. each)
- 42 lectures
- 20 labs (select labs featured during class, attendees can choose additional take-home exercises)

Course Part Number – FPGA-VDES-1-2-UFDM-COMBINED

Who Should Attend? – Hardware developers who are relatively new to Xilinx tools and technology and who still require high level QoR, and individual productivity.

Prerequisites

- None specified

Software Tools

- Vivado Design Suite

Hardware

- Architecture: Xilinx 7-Series and Ultra-Scale FPGA families

After completing this comprehensive training, you will have the necessary skills to:

- Create projects in Vivado DS
- Optimize synthesis and implementation
- Using graphical analysis tools within Vivado DS
- Fully and properly constrain design for STA
- Incorporate, generate and re-use IP cores
- Understand key Vivado reports for design analysis
- Insert debug cores as necessary
- Configure FPGA under different scenarios
- Describe the Xilinx FPGA front-to-back design flow

Course Outline

Course Specification

Session 1

Xilinx Device Architectures

- **Introduction to FPGA Architecture, 3D ICs, SoCs, ACAPs**
  Overview of FPGA architecture, SSI technology, etc.

HDL Techniques

- **HDL Coding Techniques**
  Covers basic digital coding guidelines used in an FPGA design.

Vivado Tool Flow

- **Introduction to Vivado Design Flows**
  Introduces the Vivado design flows: the project flow and non-project batch flow.
- **Vivado Design Suite Project-based Flow**
  Introduces the project-based flow in the Vivado Design Suite: creating a project, adding files to the project, exploring the Vivado IDE, and simulating the design.

Design Analysis

- **Introduction to Vivado Reports**
  Generate Vivado timing reports to analyze failed timing paths.

Power

- **Xilinx Power Estimator Spreadsheet**
  Estimate the amount of resources and default activity rates for a design and evaluate the estimated power calculated by XPE.

Synthesis and Implementation

- **Vivado Synthesis and Implementation**
  Create timing constraints according to the design scenario and synthesize and implement the design. Optionally, generate and download the bitstream to the demo board.

Pin Planning

- **Vivado Design Suite I/O Pin Planning**
  Use the I/O Pin Planning layout to perform pin assignments.

Session 2

- **Using Tcl Commands in the Vivado DS Project Flow**
  Explains what Tcl commands are executed in a Vivado Design Suite project flow.

Timing – Basics & Intermediate

- **Introduction to Clock Constraints**
  Apply clock constraints and perform timing analysis.
- **Generated Clocks**
  Use the report clock networks report to determine if there are any generated clocks in a design.
- **I/O Constraints and Virtual Clocks**
  Apply I/O constraints and perform timing analysis.
- **Setup and Hold Violation Analysis**
  Covers what setup and hold slack are and describes how to perform input/output setup and hold analysis.
- **Clock Group Constraints**
  Apply clock group constraints for asynchronous clock domains.
- **Introduction to Timing Exceptions**
  Introduces timing exception constraints and applying them to fine tune design timing.
- **Timing Constraints Wizard**
  Use the Timing Constraints Wizard to apply missing timing constraints in a design.
- **Timing Constraints Editor**

Introduces the timing constraints editor tool to create timing constraints.

- **Timing Summary Report**
  Use the post-implementation timing summary report to sign-off criteria for timing closure.

Session 3

Clocking in the UltraScale and 7-Series Architecture

- **Clocking Resources**
  Describes various clock resources, clocking layout, and routing in a design.

Clock buffers in the UltraScale and 7-Series Architecture

- **Clock Buffers**
  Describes all clocking buffers including MMCM, BUFG, BUGCE, etc.
- **Report Clock Networks**
  Use `report clock networks` to view the primary and generated clocks in a design.

I/O in the UltraScale and 7-Series Architecture

- **I/O Logic Resources**
  Overview of I/O resources and the IOB property for timing closure.

Design Techniques

- **Synchronous Design Techniques**
  Introduces synchronous design techniques used in an FPGA design.
- **Resets**
  Investigates the impact of using asynchronous resets in a design.

Power

- **Power Analysis and Optimization Using the Vivado Design Suite**
  Use report power commands to estimate power consumption.

Configuration

- **Configuration Process**
  Reviews the FPGA configuration process, such as device power up, CRC checks, etc.

Debugging

- **HDL Instantiation Debug Probing Flow**
  Covers the HDL instantiation flow to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer.

Tcl

- **Scripting in Vivado Design Suite Project Mode**
  Explains how to write Tcl commands in the project-based flow for a design.

Session 4

IP Integrator

- **Creating and Packaging Custom IP**
  Create your own IP and package and include it in the Vivado IP catalog.
- **Using an IP Container**
  Use a core container file as a single file representation for an IP.
- **Designing with the IP Integrator**
  Use the Vivado IP integrator to create the uart_led subsystem.

Vivado IP Catalog

- **Vivado IP Flow**
  Customize IP, instantiate IP, and verify the hierarchy of your design IP.
- **Block Design Containers in the Vivado IP Integrator**
  Describes the block design container (BDC) feature and shows how to create a BDC in the IP integrator.

Debugging

- **Introduction to the Vivado Logic Analyzer**
  Overview of the Vivado logic analyzer for debugging a design.
- **Introduction to Triggering**
  Introduces the trigger capabilities of the Vivado logic analyzer.
- **Debug Cores**
  Understand how the debug hub core is used to connect debug cores in a design.

UltraFast Design Methodology

- **UltraFast Design Methodology: Board and Device Planning**
  Introduces the methodology guidelines covered in this course and the UltraFast Design Methodology checklist.

UltraFast Design Methodology

- **UltraFast Design Methodology: Design Creation**
  Overview of the methodology guidelines covered in this course.

AVAILABLE LABS

- **Vivado Design Suite Project-based Flow**
- **Basic Design Analysis in the Vivado IDE**
- **Vivado Design Rule Checks *(Featured)***
- **Xilinx Power Estimator Spreadsheet**
- **Vivado Synthesis and Implementation**
- **Vivado IP Flow**
- **Vivado Design Suite I/O Pin Planning**
- **Introduction to Clock Constraints**
- **I/O Constraints and Virtual Clocks *(Featured)***
- **Timing Constraints Wizard**
- **Introduction to the Tcl Environment**
- **Resets**
- **Clocking Resources**
- **Creating and Packaging Custom IP**
- **Designing with the IP Integrator *(Featured)***
- **Design Tool Flow**
- **Introduction to Timing Exceptions**
- **Power Analysis and Optimization Using the Vivado Design Suite**
- **HDL Instantiation Debug Probing Flow**
- **Scripting in Vivado Design Suite Project Mode**
- **Design Analysis Using Tcl Commands *(Featured)***