Designing for Performance
FPGA 2

Course Outline
Day 1
- Review of Essentials of FPGA Design
- Designing with FPGA Resources
- CORE Generator Software System
- Clocking Resources
- Lab 1: Designing With FPGA Resources
- FPGA Design Techniques

Lab Descriptions
- Lab 1: Designing with FPGA Resources – Create block RAM and clocking FPGA cores using the CORE Generator™ tool. Instantiate these cores and other clock resources and implement the design.
- Lab 2: Synthesis Techniques – Experiment with different synthesis options (including timing constraints, resource sharing, synthesis optimization effort, and register balancing) and view the results.
- Lab 3: Review of Global Timing Constraints – Use the Constraints Editor to enter global timing constraints.
- Lab 4: Achieving Timing Closure – Review timing reports and enter path-specific timing constraints to fully describe your performance requirements.
- Lab 5: Designing for Performance – Improve performance and maximize results solely with implementation options and the multiple run feature.
- Lab 6: FPGA Editor Demo (optional) – Use the FPGA Editor to view a design and add a probe to an internal net.
- Lab 7: ChipScope Pro Software (optional) – Add an internal logic analyzer to a design to perform real-time debugging.

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