Zynq SoC System Architecture

Embedded Architect 3

EMBD-ZSA (v1.0)

Course Specification

Course Description

Provides experiences system architects with the knowledge on how to best architect a Zynq® System on a Chip (SoC) device project.

This course covers:

- Identifying the features and benefits of the Zynq SoC architecture
- Describing the architecture of the Arm® Cortex™-A9 processor-based processing system (PS) and the connections to the programmable logic (PL)
- Detailing the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupts, and memory controllers
- Effectively accessing and using the PS DDR controller from PL user logic
- Interfacing PL-to-PS connections efficiently
- Employing best practice design techniques for implementing functions in the PS or PL

What's New for 2020.1

- All labs have been updated to the latest software versions

Level – Embedded Architect 3

Course Details

- 2 days
  - 28 lectures
  - 10 labs
  - 8 demos

Price –

Course Part Number – EMBD-ZSA

Who Should Attend? – System architects who are interested in architecting a system on a chip using the SoC.

Prerequisites

- Digital system architecture design experience
- Basic understanding of microprocessor architecture
- Basic understanding of C programming
- Basic HDL modeling experience

Software Tools

- Vivado® Design Suite 2020.1
- Vitis™ unified software platform 2020.1

Hardware

- Architecture: Zynq-7000 SoC*
- Demo board: Zynq-7000 SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 SoC. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq SoC processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq SoC
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Course Outline

Day 1

- **Overview**
  Provides a general overview of the Zynq SoC. {Demo}
- **Application Processor Unit (APU)**
  Explores the individual components that comprise the APU. {Lab}
- **Neon Co-Processor**
  Describes the Neon co-processor that is the companion to each Cortex-A9 processor.
- **Input/Output Peripherals**
  Introduces the components that comprise the IOP block of the Zynq device PS. {Demo}
- **PS Peripherals**
  - Low-Speed: Overview: Introduces the low-speed peripherals in the Zynq SoC. {Lab}
  - Low-Speed: UART: Introduces the UART low-speed peripheral. {Demo}
  - Low-Speed: CAN: Introduces the CAN low-speed peripheral. {Demo}
  - Low-Speed: I2C: Introduces the I2C low-speed peripheral.
  - Low-Speed: SD/SDIO: Introduces the SD/SDIO low-speed peripheral.
  - Low-Speed: SPI: Introduces the SPI low-speed peripheral.
  - Low-Speed: GPIO: Introduces the GPIO low-speed peripheral.
  - High-Speed: USB: Introduces the USB high-speed peripheral.
  - High-Speed: Gigabit Ethernet: Introduces the Gigabit Ethernet high-speed peripheral. {Lab}
- **DMA Controller (DMAC)**
  Explores the operation of the DMAC, which is located in the APU. {Lab}
- **DMA**
  - Introduction and Features: Introduces the direct memory access controller.
  - Block Design and Interrupts: Introduces the DMA block design and the DMA interrupts.
  - Read and Write: Introduces the concepts behind DMA reading and writing.

Day 2

- **AXI**
  - Introduction: Introduces the AXI protocol.
  - Variations: Describes the differences and similarities among the three primary AXI variations.
  - Transactions: Describes different types of AXI transactions. {Demo, Lab}
- **PS-PL Interface**
  Describes in detail the PS interconnect and how it affects PL architecture decisions. {Demo, Lab}
- **Memory Resources**
  Explains the operation of the on-chip (OCM) memory and various memory controllers located in the PS. {Demo}
- **Booting**
  Explains the boot process of the PC and configuration of the PL. {Lab}
- **Meeting Performance Goals**
  Focuses on Zynq device performance, including DDR access from the PL, DMA considerations, and power control and reduction techniques. {Lab}

- **Hardware Design**
  Discusses the use and configuration of the PS in a hardware design.
- **Software Design**
  Explores the software side of the Zynq device. {Demo, Lab}
- **Debugging**
  Introduces debug tools and methodology on the Zynq SoC. {Lab}
- **Tools and Reference Designs**
  Describes Xilinx-provided reference design platforms, use cases, and third-party operating systems and tools for the Zynq SoC.

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