XILINX

FPGA-VAXDC4ISE-ILT (v1.0)   **Course Specification**

Course Description

This course will update experienced ISE® software users to utilize the Vivado® Design Suite. Learn the underlying database and static timing analysis (STA) mechanisms. Utilize Tcl for navigating the design, creating Xilinx design constraints (XDC), and creating timing reports. Learn to make appropriate timing constraints for SDR, DDR, source-synchronous, and system-synchronous interfaces for your FPGA design.

You will also learn to make path-specific, false path, and min/max timing constraints, as well as learn about timing constraint priority in the Vivado timing engine. Finally, you will learn about the scripting environment of the Vivado Design Suite and how to use the project-based scripting flow.

You will also learn the FPGA design best practices and skills to be successful using the Vivado Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with an UltraFast™ design methodology case study. The UltraFast design methodology checklist is also introduced.

Level – FPGA 2

Course Duration – 2 days

Course Part Number – FPGA-VAXDC4ISE-ILT

Who Should Attend? – Existing Xilinx ISE Design Suite FPGA designers

Prerequisites

- Completion of the *Vivado Design Suite for ISE Project Navigator Users* course is strongly recommended.
- Working HDL knowledge (VHDL or Verilog)
- Digital Design Experience

Optional Video

- Basic HDL Coding Techniques

Software Tools

- Vivado Design or System Edition 2018.1

Hardware

- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board: None*

* This course focuses on the UltraScale and 7 series architectures. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Create appropriate clock and input, output delay constraints and describe timing reports that involve input and output paths
- Analyze different timing reports
- Define a properly constrained design
- Describe setup and hold checks and describe the components of a timing report
- Identify key areas to optimize your design to meet your design goals and performance objectives
- Describe all of the options available with the `report_timing` and `report_timing_summary` commands
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Describe the timing constraints required to constrain system-synchronous and source-synchronous interfaces
- Identify timing closure techniques using the Vivado® Design Suite
- Describe how the UltraFast design methodology techniques work effectively through case studies and lab experiences

Course Outline

Day 1

- Introduction to Clock Constraints {Lecture, Lab, Demo}
- Generated Clocks {Lecture, Demo}
- Report Clock Networks {Lecture, Demo}
- Clock Group Constraints {Lecture, Demo}
- I/O Constraints and Virtual Clocks {Lecture, Lab}
- Timing Constraints Wizard {Lecture, Lab}
- Introduction to Vivado Reports {Lecture, Demo}
- Setup and Hold Timing Analysis {Lecture}
- Timing Summary Report {Lecture, Demo}
- Report Clock Interaction {Lecture, Demo}
- Introduction to Timing Exceptions {Lecture, Lab, Demo}
- Timing Constraints Priority {Lecture}

Day 2

- Synchronization Circuits {Lecture, Lab, Case Study}
- Report Datasheet {Lecture, Demo}
- UltraFast Design Methodology: Implementation {Lecture}
- Baselining {Lecture, Lab, Demo}
- Pipelining {Lecture, Lab}
- I/O Timing Scenarios {Lecture}
- System-Synchronous I/O Timing {Lecture, Demo}
- Source-Synchronous I/O Timing {Lecture, Lab}
- Introduction to Floorplanning {Lecture}
- Congestion {Lecture}
- Physical Optimization {Lecture, Lab}
- UltraFast Design Methodology: Design Closure {Lecture}

Topic Descriptions

Day 1

- Introduction to Clock Constraints – Apply clock constraints and perform timing analysis.
- Generated Clocks – Use the report clock networks report to determine if there are any generated clocks in a design.
- Report Clock Networks – Use report clock networks to view the primary and generated clocks in a design.
- Clock Group Constraints – Apply clock group constraints for asynchronous clock domains.
- I/O Constraints and Virtual Clocks – Apply I/O constraints and perform timing analysis.
- Timing Constraints Wizard – Use the Timing Constraints Wizard to apply missing timing constraints in a design.
- Introduction to Vivado Reports – Generate and use Vivado timing reports to analyze failed timing paths.
- Setup and Hold Timing Analysis – Understand setup and hold timing analysis.
- Timing Summary Report – Use the post-implementation timing summary report to sign-off criteria for timing closure.
- Report Clock Interaction – Use the clock interaction report to identify interactions between clock domains.
- Introduction to Timing Exceptions – Introduces timing exception constraints and applying them to fine tune design timing.
- Timing Constraints Priority – Identify the priority of timing constraints.

Day 2

- Synchronization Circuits – Use synchronization circuits for clock domain crossings.
- Report Datasheet – Use the datasheet report to find the optimal setup and hold margin for an I/O interface.
- UltraFast Design Methodology: Implementation – Introduces the methodology guidelines covered in this course.
- Baselining – Use Xilinx-recommended baselining procedures to progressively meet timing closure.
- Pipelining – Use pipelining to improve design performance.
- I/O Timing Scenarios – Overview of various I/O timing scenarios, such as source- and system-synchronous, direct/MMCM capture, and edge/center aligned data.
- System-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a system-synchronous input interface.
- Source-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a source-synchronous, double data rate (DDR) interface.
- Introduction to Floorplanning – Introduction to floorplanning and how to use Pblocks while floorplanning.
- Congestion - Identifies congestion and addresses congestion issues.
- Physical Optimization – Use physical optimization techniques for timing closure.
- UltraFast Design Methodology: Design Closure – Introduces the methodology guidelines covered in this course.

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