UltraScale and UltraScale+ Architectures Workshop

FPGA 3

FPGA-US1D (v1.0)

Course Specification

Course Description

This is a one-day version of the *Designing with the UltraScale and UltraScale+ Architectures* course and introduces new and experienced designers to the most sophisticated aspects of the UltraScale™ and UltraScale+™ architectures. Targeted towards designers who have used the Vivado® Design Suite, this course focuses on designing for the new and enhanced resources found in our newest FPGA family.

Topics covered include an introduction to the clock management resources (MMCM and PLL), global and regional clocking resources, memory resources, and source-synchronous resources. A description of the improvements to the dedicated transceivers and Transceiver Wizard is also included. Use of the Memory Interface Generator (MIG) and the new DDR4 memory interface capabilities is also covered.

In addition, you will learn how to best migrate your design and IP to the UltraScale architecture and the best way to use the Vivado Design Suite during design migration. A combination of modules and labs allow for practical hands-on experience of the principles taught.

What's New for 2021.1

- All labs have been updated to the latest software versions

Level – FPGA 3

Course Details

- 1 day
  - 14 lectures
  - 8 labs
  - 1 demo

Price –

Course Part Number – FPGA-US1D

Who Should Attend? – Anyone who would like to build a design for the UltraScale or UltraScale+ device family

Prerequisites

- *Designing FPGAs Using the Vivado Design Suite 1* course
- Intermediate VHDL or Verilog knowledge

Software Tools

- Vivado HL Design or System Edition 2021.1

Hardware

- Architecture: UltraScale and UltraScale+ FPGAs*
- Demo board: None*

* This course focuses on the UltraScale and UltraScale+ architectures. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Take advantage of the primary UltraScale architecture resources
- Define the block RAM and FIFO resources available for UltraScale FPGAs
- Describe the UltraRAM features
- Properly design for the I/O and SERDES resources
- Identify the MMCM, PLL, and clock routing resources included with the UltraScale architecture
- Identify the hard IP resources available for implementing high-performance DDR4 physical layer interfaces
- Describe the additional features of the dedicated transceivers
- Effectively migrate your IP and design to the UltraScale architecture as quickly as possible

Course Outline

- **UltraScale Architecture CLB Resources**
  Examine the CLB resources, such as the LUT and the dedicated carry chain, in the UltraScale architecture. {Lecture, Lab}
- **UltraScale Architecture Clocking Resources**
  Use the Clocking Wizard to configure a clocking subsystem to provide various clock outputs and distribute them on the dedicated global clock networks. {Lectures, Lab}
- **FPGA Design Migration**
  Migrate an existing 7 series design to the UltraScale architecture. {Lecture, Lab}
- **UltraScale Architecture Block Memory Resources**
  Review the block RAM resources in the UltraScale architecture. {Lecture}
- **UltraScale Architecture FIFO Memory Resources**
  Review the FIFO resources in the UltraScale architecture. {Lecture}
- **UltraRAM Memory**
  Use UltraRAM for a design requiring a larger memory size than block RAM. {Lecture, Lab}
- **DDR4 Design Creation Using MIG**
  Create a DDR4 memory controller with the Memory Interface Generator (MIG) utility. {Lab}
- **UltraScale Architecture I/O Resources Overview**
  Provides an overview of the I/O resources in the UltraScale architecture. {Lecture}
- **UltraScale Architecture I/O Resources: Component Mode**
  Implement a high-performance, source-synchronous interface using I/O resources in Component mode for the UltraScale architecture. {Lecture, Lab}
- **UltraScale Architecture I/O Resources: Native Mode**
  Implement a high-performance, source-synchronous interface using I/O resources in Native mode for the UltraScale architecture. {Lecture, Lab}
- **UltraScale Architecture Transceivers**
  Review the enhanced features of the transceivers in the UltraScale architecture. {Lecture}
- **UltraScale FPGAs Transceivers Wizard**
  Use the Transceivers Wizard to build a design that uses a single serial transceiver and observe the created file structures. {Lecture, Lab}

Register Today

Visit the Xilinx Customer Training Center to view schedules and register online.