Timing Closure Techniques

FPGA 2

FPGA-ADVTIMING (v1.0)

Course Specification

Course Description

Learn how to apply UltraFast Design Methodology timing closure techniques and to achieve timing closure for a given design.

The emphasis of this course is on:

- Applying initial design checks and reviewing timing summary and methodology reports for a design
- Using baselining to verify that a design meets timing goals and applying the guidelines described in the baselining process
- Identifying and resolving setup and hold violations
- Reducing logic delays, net delays, and congestion in a design
- Improving clock skew and clock uncertainty
- Performing Pblock-based and super logic region (SLR)-based analysis to identify challenges and improve timing closure
- Performing quality of results (QoR) assessments at different stages to improve the QoR score
- Implementing Intelligent Design Runs (IDR) to automate analysis and timing closure for complex designs

Level – FPGA 2

Course Details

- 2 days ILT
  - 11 lectures
  - 6 labs

Price –

Course Part Number – FPGA-ADVTIMING

Who Should Attend? – Software and hardware developers, system architects, and anyone who wants to learn about UltraFast Design Methodology timing closure techniques

Prerequisites

- Basic knowledge of FPGA and SoC architecture and HDL coding techniques
- Basic knowledge of the Vivado® Design Suite

Software Tools

- Vivado Design Suite 2021.2

Hardware

- Architecture: UltraScale™ FPGAs and Versal® ACAPs

After completing this comprehensive training, you will have the necessary skills to:

- Describe UltraFast Design Methodology timing closure techniques
- Resolve setup and hold violations
- Reduce logic delay and net delay
- Reduce congestion
- Improve clock skew and clock uncertainty
- Perform Pblock-based and SLR-based analysis
- Identify clock domain crossings (CDC) and scenarios that require synchronization circuits
- Perform QoR assessment at different stages and improve the QoR score
- Implement Intelligent Design Runs (IDR)

Course Outline

Day 1

Static Timing Analysis

- **Introduction to Clocking and Static Timing Analysis (STA)**
  Describes the basics of clock gating, static timing analysis, and setup and hold slack. {Lecture}

UltraFast Design Methodology Timing Closure

- **Introduction to UltraFast Design Methodology Timing Closure**
  Provides an overview of the various stages of the UltraFast Design Methodology for timing closure. {Lecture}

Baselining

- **Baselining**
  Demonstrates the performance baselining process, which is an iterative approach to incrementally constrain a design and meet timing. {Lecture, Lab}

Design Analysis and Optimization

- **Setup and Hold Violation Analysis**
  Covers what setup and hold slack are and describes how to perform input/output setup and hold analysis. {Lecture}
- **Reducing Logic Delay**
  Describes how to optimize regular fabric paths and paths with dedicated blocks and macro primitives. {Lecture}
- **Reducing Net Delay**
  Reviews different techniques to reduce congestion and net delay. {Lecture, Lab}

Day 2

Design Analysis and Optimization (Continue)

- **Improving Clock Skew**
  Describes how to apply various techniques to improve clock skew. {Lecture}
- **Improving Clock Uncertainty**
  Reviews various flows for improving clock uncertainty, including using parallel BUFGCE_DIV clock buffers, changing MMCM or PLL settings, and limiting synchronous clock domain crossing (CDC) paths. {Lecture, Lab}

Clock Domain Crossing (CDC)

- **Clock Domain Crossing (CDC) and Synchronization Circuits**
  Explains what clock domain crossings (CDC) are and the scenarios that require synchronization circuits. {Lecture, Lab}

Report QoR

- **QoR Reports Overview**
  Describes what quality of result (QoR) is and how to analyze the QoR reports generated by the Vivado IDE. {Lecture, Lab}

Design Runs

- **Intelligent Design Runs (IDR)**
  Introduces Intelligent Design Runs (IDR), which are special types of implementation runs that use a complex flow to attempt to close timing. {Lecture, Lab}