Signal Integrity and Board Design for Xilinx FPGAs

Connectivity 3

CONN-SI-ILT (v1.0)

Course Specification

Course Description

Learn when and how to apply signal integrity techniques to high-speed interfaces between Xilinx FPGAs and other components. This comprehensive course combines design techniques and methodology with relevant background concepts of high-speed bus and clock design, including transmission line termination, loading, and jitter.

You will work with IBIS models and complete simulations using Mentor Graphics HyperLynx. Other topics include managing PCB effects and on-chip termination. This course balances lecture modules with instructor demonstrations and practical hands-on labs.

Level – Connectivity 3

Course Duration – 3 days

Price –

Course Part Number – CONN-SI-ILT

Who Should Attend? – Digital designers, board layout designers, or scientists, engineers, and technologists seeking to implement Xilinx solutions. Also end users of Xilinx products who want to understand how to implement high-speed interfaces without incurring the signal integrity problems related to timing, crosstalk, and overshoot or undershoot infractions.

Prerequisites

- FPGA design experience preferred (*Designing FPGAs Using the Vivado Design Suite 1* course or equivalent)
- Familiarity with high-speed PCB concepts
- Basic knowledge of digital and analog circuit design
- Vivado™ tool knowledge is helpful

Software Tools

- Vivado System Edition 2012.4
- Mentor Graphics HyperLynx 8.2.1

Hardware

- Architecture: N/A*
- Demo board: None*

* This course does not focus on any particular architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe signal integrity effects
- Predict and overcome signal integrity challenges
- Simulate signal integrity effects
- Verify and derive design rules for the board design
- Apply signal integrity techniques to high-speed interfaces between Xilinx FPGAs and semiconductor circuits
- Plan your board design under FPGA-specific restrictions
- Supply the FPGAs with power
- Handle thermal aspects

Course Outline

Part 1 – Signal Integrity

- Signal Integrity Introduction
- Transmission Lines
- IBIS Models and SI Tools
- **Lab 1:** Invoking HyperLynx
- Reflections
- **Lab 2:** Reflection Analysis
- Crosstalk
- **Lab 3:** Crosstalk Analysis
- Signal Integrity Analysis
- Power Supply Issues
- Signal Integrity Summary

Part 2 – Board Design

- Board Design Introduction
- FPGA Power Supply
- **Lab 4:** Power Analysis
- FPGA Configuration and PCB
- Signal Interfacing: Interfacing in General
- Signal Interfacing: FPGA-Specific Interfacing
- **Lab 5:** I/O Pin Planning
- Die Architecture and Packaging
- PCB Details
- Thermal Aspects
- **Lab 6:** Thermal Design
- Tools for PCB Planning and Design
- Board Design Summary

Lab Descriptions

- **Lab 1:** Invoking HyperLynx – Become familiar with signal integrity tools. Use HyperLynx for schematic entry, modeling, and simulation. Modify a standard IBIS model to define a driver and then use its stackup editor to define a PCB.
- **Lab 2:** Reflection Analysis – Define a circuit and run various simulations for effects of reflection.
- **Lab 3:** Crosstalk Analysis – Using simulation, analyze circuit topology and PCB data for strategies to minimize crosstalk.
- **Lab 4:** Power Analysis – Estimate initial power requirements using an Excel spreadsheet, then use the Vivado Power Analyzer to accurately predict board power needs.
- **Lab 5:** Pin Planning – Use the PlanAhead software to identify pin placement and implement pin assignments.
- **Lab 6:** Thermal Design – Determine maximum junction temperature and calculate acceptable thermal resistance.

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