SDSoC Development Environment and Methodology

Embedded 2

EMBD-SDSOC (v1.0)

Course Specification

Course Description

Designers new to the SDSoC™ development environment will learn how, using the full tool flow, to either create an accelerated system or accelerate an existing design at the system architecture level.

The focus is on:

- Identifying functions for hardware acceleration
- Debugging functions
- Moving software functions into hardware and estimating performance
- Utilizing hardware/software event tracing

Several optional modules are also provided to quickly provide students with the necessary background on both hardware and software.

Level – Embedded 2

Course Duration – 1 day

Price –

Course Part Number – EMBD-SDSOC

Who Should Attend? – Anyone interested in quickly adding hardware acceleration to a software system.

Prerequisites

- Understanding of Zynq®-7000 architecture (with emphasis on ACP, HP ports, and internal routing)
- Comfort with the C, C++ programming language
- Familiarity with the Vivado® Design Suite, Vivado HLS tool, and Xilinx SDK

Software Tools

- SDx™ development environment 2018.3

Hardware

- Architecture: Zynq-7000 SoC*
- Demo board: Zynq-7000 SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 SoC. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify candidate functions for hardware acceleration by using the TCF profiling tool
- Use the System Debugger's capabilities to control the execution flow and examine memory and variables during a debug session
- Move designated software functions to hardware and estimate the performance of the accelerator and the effect on the entire system
- Use the hardware/software event trace to understand the performance of an application given the workload, hardware/software partitioning, and system design choices

Course Outline

- Zynq SoC Architecture Support for Accelerators [Optional]
- Zynq UltraScale+ MPSoC Architecture Support for Accelerators [Optional]
- Software Overview [Optional]
- Introduction to the SDSoC Tool {Lecture}
- SDSoC Tool Flow {Lecture, Demo, Lab}
- Application Debugging {Lecture, Demo, Lab}
- Application Profiling {Lecture, Demo, Lab}
- Understanding Estimations in the SDSoC Tool {Lecture, Demo, Lab}
- QEMU Emulation {Lab}
- Hardware/Software Event Tracing {Lecture, Lab}

Topic Descriptions

- Zynq SoC Architecture Support for Accelerators [Optional] – Discusses the relevant aspects of the Zynq SoC architecture for accelerator design. The focus is on AXI ports and protocols, system latency, and memory utilization.
- Zynq UltraScale+ MPSoC Architecture Support for Accelerators [Optional] – Discusses the relevant aspects of the Zynq UltraScale+ MPSoC architecture for accelerator design.
- Software Overview [Optional] – Provides a thorough understanding of how the integrated design environment works, including how the compiler and linker behave, basics of makefiles, DMA usage, and variable scope.
- Introduction to the SDSoC Tool {Lecture} – Introduces the purpose, underlying structures, and basic functionality of the SDSoC development environment.
- SDSoC Tool Flow {Lecture, Demo, Lab} – Explains the complete development flow of the SDSoC integrated development environment (IDE).
- Application Debugging {Lecture, Demo, Lab} – Through the use of the System Debugger, students will learn how to follow the control flow in an executing application and see the effects of the code on memory to successfully debug software issues.
- Application Profiling {Lecture, Demo, Lab} – Profiling is the process that identifies how the processor is spending its time. Through profiling, the user can quickly identify which functions must be optimized or moved to hardware to satisfy the performance requirements.
- Understanding Estimations in the SDSoC Tool {Lecture, Demo, Lab} – Once a function is moved to hardware, questions remain: Will the accelerator fit in hardware? Will it fun fast enough? Estimations can provide the answers.
- QEMU Emulation {Lab} – Describes how to use the emulation feature in the SDx IDE.
- Hardware/Software Event Tracing {Lecture, Lab} – Hardware/software event tracing helps users understand the performance of their application given the workload, hardware/software partitioning, and system design choices. Such information helps the user to optimize and improve system implementation.

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