# PCIe Protocol Overview

Connectivity 2

PCIE18000-13-ILT (v1.0)

**Course Specification**

## Course Description

This course focuses on the fundamentals of the PCI Express® protocol specification. The typical PCIe architecture, including data space, data movement, and the most commonly used Transaction Layer Packets (TLPs) are covered. Interrupts and error handling are also discussed.

Implementation issues are covered in the two-day *Designing a LogiCORE PCI Express System* course.

**Level** – Connectivity 2

**Course Duration** – 1 day

**Price** –

**Course Part Number** – PCIE18000-13-ILT

**Who Should Attend?** – FPGA designers, logic designers, and anyone who needs an in-depth knowledge of the PCIe protocol

**Prerequisites**

- None

**Software Tools**

- None required
- VCD viewer optional

**Hardware**

- Architecture: N/A*
- Demo board: None*

* This course does not focus on any particular architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Interpret various transactions occurring on the link
- Describe the layered architecture and the tasks and packet types each is responsible for
- Properly estimate maximum performance of a link
- Illustrate how errors can be communicated within the system
- Explain the relationship between Virtual Channels (VCs) and Traffic Class (TC) and the interaction with flow control credits

## Course Outline

- Introduction
- Introduction to the PCIe Architecture
- Review of the PCIe Protocol
- Packet Formatting Details
- **Lab 1:** Packet Decoding
- Packet Routing
- Interrupts and Error Management
- Summary

## Lab Descriptions

- **Lab 1:** Packet Decoding – This lab explores what *really* happens on the link between a root complex and the endpoint. Various packets, including the Physical Layer, Data Link Layer, and Transaction Layer packets are explored. Insight as to what is actually transpiring on the lanes becomes a powerful tool for understanding the protocol as well as debugging various link issues.

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