DSP-ESS (v1.0)

Course Specification

Course Description

This course provides a foundation for digital signal processing (DSP) techniques for Xilinx devices.

The emphasis is on:

- Reviewing basic binary number theory, mathematics, and the essential features within the FPGA that are important to signal processing
- Exploring a variety of filter techniques with a focus on optimal implementation in Xilinx devices and continues with an examination of FFTs, video, and image processing.
- Introducing Xilinx cores and IP that are relevant to signal processing

Level – DSP 3

Course Duration – 2 days

Price –

Course Part Number – DSP-ESS

Who Should Attend? – Engineers and designers who have an interest in developing products that use digital signal processing

Prerequisites

A fundamental understanding of digital signal processing theory, including an understanding of the following principles:

- Sample rates
- Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters
- Oscillators and mixers
- Fast Fourier Transform (FFT) algorithm

Recommended

- *Designing with FPGAs Using the Vivado Design Suite 1* course

Hardware

- Architecture: 7 series FPGAs*
- Demo board: None*

* This course focuses on the 7 series FPGA architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the advantages of using FPGAs over traditional processors for DSP designs
- Utilize fixed point binary arithmetic and identify how to use this knowledge to create efficient designs in FPGAs
- Recognize how both the CLB slices in FPGAs and the more advanced DSP48s are used to implement DSP algorithms
- Explain the dataflow through the device and how to use distributed memory, block RAM, registers, and SRLs to properly implement these designs
- Construct different FIR filter and FFT implementations and how to optimize these implementations in the FPGA
- Explain the algorithms for video and imaging systems and their implementations in FPGAs

Course Outline

Day 1

- Back to Basics
- Architecture

- FPGA Math
- **Exercise 1:** Signed Number Conversion, Quantization and Rounding, Adders, Subtractors, and Accumulation
- Shift Registers, RAM, and Applications
- **Exercise 2:** SRL32E and RAM Estimation and Concatenation
- FIR Filter
- **Exercise 3:** Filter Implementation, Resource and Performance Estimation

Day 2

- Advanced Filter Techniques
- **Exercise 4:** Filter Implementations, Resource and Performance Estimation
- Fast Fourier Transform
- **Exercise 5:** FFT Implementation, Resource and Performance Estimation
- Video and Imaging
- Where Do We Go From Here?
- **Demonstration:** System Generator and the CORE Generator Tool with a DSP-Targeted Reference Design
- Where Can I Learn More?

Lab Descriptions

- **Exercise 1:** Signed Number Conversion, Quantization and Rounding, Adders, Subtractors, and Accumulation – Learn how to estimate device resource utilization for basic math functions. Compare different methodologies for implementing functions.
- **Exercise 2:** SRL32E and RAM Estimation and Concatenation – Learn how to optimize memory and storage in Xilinx FPGAs.
- **Exercise 3:** Filter Implementation, Resource and Performance Estimation – Learn how and when to use various implementation strategies for optimal filter implementation.
- **Exercise 4:** Filter Implementations, Resource and Performance Estimation – Advanced filter topologies are studied. Architect multichannel and multirate filters using various methods. Implementation strategies will be discussed and optimal methods used.
- **Exercise 5:** FFT Implementation, Resource and Performance Estimation – Select correct parameters for FFT implementations to meet design targets. Resource estimation will be studied and trade-offs with performance examined through implementation examples.
- **Demonstration:** System Generator and the CORE Generator Tool with a DSP-Targeted Reference Design – Introduces DSP-targeted hardware boards and software tools. Witness the power, ease of use, and design efficiency of Xilinx DSP tools and IP. Reinforce the concepts studied in the course material and exercises.

Register Today

Visit the Xilinx Customer Training Center to view schedules and register online.