Course Description

Learn general embedded concepts, tools, and techniques using the Vivado® Design Suite and Vitis™ unified software platform.

The emphasis is on:

- Designing, expanding, and modifying embedded systems utilizing the features and capabilities of the Zynq® System on a Chip (SoC), Zynq UltraScale+™ MPSoC, or MicroBlaze™ soft processor
- Adding and simulating AXI-based peripherals using bus functional model (BFM) simulation

What's New for 2021.2

- All labs have been updated to the latest software versions

Level – Embedded Hardware 3

Course Details

- 2 days ILT
    - 17 lectures
    - 8 labs
    - 6 ILT demos

Price –

Course Part Number – EMBD-HW

Who Should Attend? – Engineers who are interested in developing embedded systems with the Xilinx Zynq SoC, Zynq UltraScale+ MPSoC, and/or MicroBlaze soft processor core

Prerequisites

- FPGA design experience
- Completion of the *Designing FPGAs Using the Vivado Design Suite 1* course or equivalent knowledge of Xilinx Vivado software implementation tools
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some HDL modeling experience

Software Tools

- Vivado Design Suite 2021.2
- Vitis unified software platform 2021.2

Hardware

- Architectures: Zynq-7000 SoC (Cortex™-A9 processor), Zynq UltraScale+ MPSoC (Cortex-A53 and Cortex-R5 processors), and MicroBlaze processor*
- Demo board: Zynq UltraScale+ MPSoC ZCU104 or Versal® ACAP VCK190 board*

* This course focuses on the Zynq-7000 SoC and Zynq UltraScale+ MPSoC architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the various tools that encompass a Xilinx embedded design
- Rapidly architect an embedded system containing a Cortex-A9/A53/R5 or MicroBlaze processor using the Vivado IP integrator and Customization Wizard
- Develop software applications utilizing the Vitis unified software platform

Course Specification

- Create and integrate an IP-based processing system component in the Vivado Design Suite
- Design and add a custom AXI interface-based peripheral to the embedded processing system
- Simulate a custom AXI interface-based peripheral using verification IP (VIP)

Course Outline

Day 1

- **Embedded UltraFast Design Methodology**
  Outlines the different elements that comprise the Embedded Design Methodology. {Lecture, Demo}
- **Overview of Embedded Hardware Development**
  Overview of the embedded hardware development flow. {Lecture, Demo}
- **Driving the IP Integrator Tool**
  Describes how to access and effectively use the IPI tool. {Lecture, Lab}
- **Overview of Embedded Software Development**
  Reviews the process of building a user application. {Lecture}
- **Driving the Vitis Software Development Tool**
  Introduces the basic behaviors required to drive the Vitis tool to generate a debuggable C/C++ application. {Lecture, Lab}
- **AXI: Introduction**
  Introduces the AXI protocol. {Lecture}
- **AXI: Variations**
  Describes the differences and similarities among the three primary AXI variations. {Lecture}
- **AXI: Transactions**
  Describes different types of AXI transactions. {Lecture, Demo, Lab}
- **Introduction to Interrupts**
  Introduces the concept of interrupts, basic terminology, and generic implementation. {Lecture}
- **Interrupts: Hardware Architecture and Support**
  Reviews the hardware that is typically available to help implement and manage interrupts. {Lecture}

Day 2

- **AXI: Connecting AXI IP**
  Describes the relationships between different types of AXI interfaces and how they can be connected to form hierarchies. {Lecture, Demo}
- **Creating a New AXI IP with the Wizard**
  Explains how to use the Create and Import Wizard to create and package an AXI IP. {Lecture, Lab}
- **AXI: BFM Simulation Using Verification IP**
  Describes how to perform BFM simulation using the Verification IP. {Lecture, Lab}
- **MicroBlaze Processor Architecture Overview**
  Overview of the MicroBlaze microprocessor architecture. {Lecture, Lab}
- **MicroBlaze Processor Block Memory Usage**
  Highlights how block RAM can be used with the MicroBlaze processor. {Lecture}

EMBD-HW (v1.0) updated February 2022
Course Specification
www.xilinx.com
1-800-255-7778

- **Zynq-7000 SoC Architecture Overview**

  Overview of the Zynq-7000 SoC architecture. {Lecture, Demo, Lab}

- **Zynq UltraScale+ MPSoC Architecture Overview**

  Overview of the Zynq UltraScale+ MPSoC architecture. {Lecture, Demo, Lab}

Register Today

Visit the Xilinx Customer Training Center to view schedules and register online.