Developing Multimedia Solutions with the Video Codec Unit Using the GStreamer Framework

MMEDIA 3

EMBD-MMEDIA (v1.0)

Course Specification

Course Description

Learn how to build and run complex multimedia applications targeting Zynq® UltraScale+™ MPSoC EV devices with the help of the GStreamer framework. This course also illustrates how the use of the hardened video codec unit in the EV device helps to achieve optimum performance by offloading critical tasks to the dedicated processing engines.

The emphasis of this course is on:

- Describing the multimedia solutions provided by Xilinx
- Developing a multimedia application targeting Zynq UltraScale+ MPSoC EV devices
- Listing the multimedia hardened blocks available in Zynq UltraScale+ MPSoC EV devices
- Explaining the encoder and decoder functionalities of a video codec unit
- Describing the software stack provided by Xilinx for developing multimedia applications
- Describing the Vitis Video Analytics SDK (VVAS) technology
- Utilizing the GStreamer framework from the software stack to create different multimedia pipelines

What's New for 2021.1

- New content on Vitis Video Analytics SDK (VVAS) technology (two new modules)
- New lab on multichannel ML pipeline using VVAS
- Regular updates to the content based on 2021.1 release
  - General VCU updates
  - New content on VCU region of interest (ROI) encoding
- Targeting the ZCU104 board instead of the ZCU106 in all the labs
- All labs have been updated to the latest software versions

Level – MMEDIA 3

Course Details

- 2 days ILT
  - 15 lectures
  - 5 labs

Price –

Course Part Number – EMBD-MMEDIA

Who Should Attend? – Anyone who needs to develop multimedia application targeting Zynq UltraScale+ MPSoC EV devices

Prerequisites

- Basic knowledge of video technology
- Basic knowledge of a video codec unit (VCU)
- Intermediate level of knowledge of the Zynq UltraScale+ MPSoC architecture

Software Tools

- Vivado Design Suite 2021.1
- PetaLinux Tool 2021.1

Hardware

- Zynq UltraScale+ MPSoC ZCU104 board*
- HDMI-supported display device (monitor)
- Source (Nvidia Shield or ABOX)
- Two HDMI cables and one ethernet cable

* This course focuses on Xilinx multimedia solutions. Check with your local Authorized Training Provider for the specifics of the in-class lab environment or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the multimedia solutions provided by Xilinx
- Utilize the VCU and GPU multimedia blocks in Zynq UltraScale+ MPSoC EV devices
- Perform video encoding and decoding using the hardened video codec unit (VCU)
- Describe the VCU software stack
- Use GStreamer plugins to create video pipelines
- Describe what Vitis Video Analytics SDK (VVAS) technology is
- Perform machine learning with an application using VVAS technology
- Describe the different audio, video, connectivity, and processing soft IPs from Xilinx
- Run video transcoding and video streaming applications

Course Outline

Day 1

- **Multimedia Overview {Lecture}**
  Provides an overview of multimedia components and major trends. Also describes why Xilinx is focused on multimedia.
- **Xilinx Multimedia Solutions {Lecture}**
  Provides a top-level introduction of the different multimedia solutions from Xilinx, including Zynq UltraScale+ MPSoC EV devices, multimedia blocks, the software stack, soft IPs, and tools.
- **Zynq UltraScale+ MPSoC: Multimedia Blocks {Lecture}**
  Reviews the different multimedia blocks available in Zynq UltraScale+ MPSoC EV devices, including the dedicated video codec units, graphics processors, DisplayPort controllers, and DDR controllers.
- **Introduction to Video Codec Units (VCU) {Lecture}**
  Covers the basics of a video codec unit, including why a video code is needed, what it does, and its basic components.
- **Zynq UltraScale+ MPSoC: VCU Architecture {Lecture, Lab}**
  Covers the video pipeline and reviews the Zynq UltraScale+ MPSoC EV VCU encoder and decoder architecture in detail.
- **VCU-supported Standards and VCU Latency and Performance {Lecture}**
  Discusses the VCU-supported coding standards and provides more information on VCU latency and performance. The different profiles of the H.264/AVC standard is covered in detail, and different low-latency modes are reviewed.
- **Introduction to the GStreamer Framework {Lecture, Lab}**
  Describes the GStreamer framework and its basic building blocks. Also describes the advantages of using GStreamer for multimedia application development and how GStreamer interacts with an application.
- **VCU Software Stack {Lecture}**
  Describes the VCU software stack provided by Xilinx, including the control software, OpenMAX and GStreamer layers. Control software is provided for those with their own custom frameworks and logic.

Day 2

- **Vitis Video Analytics SDK (VVAS) Overview {Lecture}**
  Provides an overview of the Vitis Video Analytics SDK (VVAS) technology, including describing its architecture and features.
- **Multimedia-supported Frameworks in Linux: V4L2, DRM, KMS, ALSA {Lecture, Lab}**
  Covers the multimedia frameworks supported in Linux (such as V4L2, DRM, KMS and ALSA) and how they are implemented in a video pipeline. The concept of buffer sharing is also discussed.
- **VVAS Core Components {Lecture, Lab}**
  Describes the GStreamer plugins and core components of VVAS technology in detail.
- **Multimedia Connectivity and Processing IPs {Lecture}**
  Reviews the different input and output subsystems that are used to capture and display audio and video data. The corresponding connectivity and processing IPs provided by Xilinx are also covered.
- **Streaming Pipeline Using GStreamer {Lecture, Lab}**
  Describes in detail the streaming pipeline application flow using GStreamer, including how to build a GStreamer application.
- **Xilinx Audio and Graphics Solutions {Lecture}**
  Provides an overview of the features of the Xilinx audio solution. Also describe the GPU architecture and functionality of the GPU software stack provided by Xilinx.
- **Xilinx Targeted Reference Designs Overview {Lecture}**
  Describes the multimedia-based Targeted Reference Designs from Xilinx. In particular, the Zynq UltraScale+ MPSoC Base TRD and Zynq UltraScale+ MPSoC VCU TRD are discussed in detail.

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