Designing with the Zynq UltraScale+ RFSoC

Connectivity 3

CONN-RFSOC (v1.0)

Course Specification

Course Description

This course provides an overview of the hard block capabilities for the Zynq® UltraScale+™ RFSoC family with a special emphasis on the RF Data Converter and Soft-Decision FEC blocks.

The focus is on:

- Describing the RFSoC family in general
- Identifying applications for the RF Data Converter and SD-FEC blocks
- Configuring, simulating, and implementing the blocks
- Verifying the RF Data Converter on real hardware
- Reviewing power estimation to help identify the power demands of the RFSoC device in various operating modes
- Identifying proper layout and PCB considerations since the Zynq UltraScale+ RFSoC is both a high-speed and an analog and digital device

What's New for 2020.1

- *Overview Modules*
  - Updated to DUAL/QUAD nomenclature
  - Updated Gen3 general parameters
  - Updated Gen3 evaluation boards
- *RF-ADC and RF-DAC Modules*
  - Updated to 2020.1 software
  - Added more functionality details
- *Data Converter Practice*
  - Added frequency planning
  - Added RF data converter design example

Level – Connectivity 3

Course Details

- 3 days ILT or 24 hours OnDemand
  - 37 lectures
  - 8 labs
  - 5 demos

Price –

Course Part Number – CONN-RFSOC

Who Should Attend? – Hardware designers interested in understanding the architecture and capabilities of the Zynq UltraScale+ RFSoC data converter and SD-FEC hard blocks.

Prerequisites

- Suggested: Understanding of the Zynq UltraScale+ MPSoC architecture
- Basic familiarity with data converter terms and principles
- Basic familiarity with forward error correction terms and principles

Software Tools

- Vivado® Design Suite 2020.1
- Vitis unified software platform [*** vitis_version_number ***]

Hardware

- Host computer for running the above software
- Zynq UltraScale+ RFSoC ZCU111 board*

* This course focuses on the Zynq UltraScale+ RFSoC architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe in general the new Zynq UltraScale+ RFSoC family
- Identify typical applications for the RF data converters
- Describe the architecture and functionality of the RF-ADC
- Utilize the RF-ADC via configuration, simulation, and implementation
- Describe the architecture and functionality of the RF-DAC
- Utilize the RF-DAC via configuration, simulation, and implementation
- Identify the requirements and options for data converter PCB designs
- Describe the architecture and functionality of the Soft-Decision FEC hard IP
- Utilize the Soft-Decision FEC via configuration, simulation, and implementation

Course Outline

- **Zynq UltraScale+ RFSoC Overview**

  Overview of the Zynq UltraScale+ RFSoC architecture, including brief introductions to RF, RF data converter solutions, SD-FEC solutions, driver support, and tool support. {Lectures, Demo}
- **RF-ADC Hardware**

  Covers the basics of RF-ADCs. Reviews RF-ADC architecture, functionality, interfaces, configuration, and driver support. {Lectures, Demo, Lab}
- **RF-DAC Hardware**

  Covers the basics of RF-DACs. Reviews RF-DAC architecture, functionality, interfaces, configuration, and driver support. {Lectures, Demo, Lab}
- **RFSoC Hardware**

  Provides an overview of the ZCU111 board and describes board setup. {Lectures}
- **Data Converter Design**

  Describes common features, the design flow, utilizing the example design by simulation and implementation, and verifying RF data converter functionality on real hardware. Includes practice of using a software driver to modify RF data converter parameters. {Lectures, Labs}
- **Data Converter Practice**

  Provides practical RF data converter experience using the ZCU111 board evaluation tool and RF analyzer tool. Demonstrates a PYNQ-based application to validate QPSK streams. Describes RF data converter frequency planning. Utilizes an RF data converter design example. {Lectures, Practices}
- **PCB Design for RFSoC Devices**

  Describes power requirements, performing power estimation, and utilizing the power design. Analog signal requirements, PCB materials and layer stackup options, and analog trace design are also covered. {Lectures, Demo, Lab}

- **Soft-Decision FEC Hardware**
  Covers the basics of forward error correction. Reviews SD-FEC architecture, functionality, interfaces, configuration, and driver support. {Lectures, Demo, Labs}

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