AMD XILINX

Designing with the Versal ACAP: PCI Express Systems

ACAP-PCIE (v1.0)

Course Specification

Course Description

This course introduces the features and capabilities of the PCIe® and Cache Coherent Interconnect blocks in the Versal® architecture. Learn how to implement a Versal ACAP PCI Express® solution in custom applications to improve time to market.

The emphasis of this course is on:

- Describing the Xilinx PCI Express design methodology
- Enumerating various Xilinx PCI Express core products
- Selecting the PCI Express IP cores from the Vivado® Design Suite
- Generating PCI Express example designs and simple applications
- Identifying the advanced capabilities of the PCIe specification

This course also focuses on the AXI-Streaming interconnect.

What's New for 2022.1

- Updates for new Versal ACAP devices
- All labs have been updated to the latest software versions

Level – Connectivity 3

Course Details

- 2 days

Course Part Number – ACAP-PCIE

Who Should Attend?

- Hardware designers who want to create applications using Xilinx IP cores for PCI Express
- Software engineers who want to understand the deeper workings of the Xilinx PCI Express solution
- System architects who want to leverage key Xilinx advantages related to performance, latency, and bandwidth in PCI Express applications

Prerequisites

- Experience with the PCI/PCIe specification protocol
- Knowledge of VHDL or Verilog
- Some experience with Xilinx implementation tools
- Some experience with a simulation tool, preferably the Vivado® simulator
- Moderate digital design experience

Software Tools

- Vivado Design Suite 2022.1

Hardware

- Architecture: Xilinx Versal ACAPs

After completing this comprehensive training, you will have the necessary skills to:

- Construct a basic PCI Express system by:
    - Selecting the appropriate IP for your application
    - Specifying requirements of an endpoint application
    - Connecting PCIe IPs with the user application
    - Utilizing PL and PS resources supporting PCI Express
    - Simulating and implementing PCI Express systems
- Identify the advanced capabilities of the PCI Express specification protocol and feature set

Course Outline

Day 1

- **Introduction to PCI Express**
  Introduces the course and discusses a few key topics of the PCI Express protocol. {Lecture, Lab}

- **Versal ACAP PCIe Solutions Overview**
  Provides an overview of the Xilinx PCI Express solutions in the Versal architecture and identifies key differentiators. {Lecture}

- **PCIe Block Architecture and Functionality**
  Describes the PL PCIe block architecture. You will learn details on the block features and functionality. {Lecture}

- **PCIe Block Interfaces Overview**
  Provides an overview of the PL PCIe block interfaces. Deeper discussion on physical layer and general interfaces. {Lecture}

- **PCIe Block Requester Interfaces**
  Reviews the requester AXI4-Streaming core interfaces. You will learn how to utilize packet descriptors for request interfaces. {Lecture}

- **PCIe Block Completer Interfaces**
  Reviews the completer AXI4-Streaming core interfaces. You will learn how to utilize packet descriptors for completion interfaces. {Lecture, Lab}

- **PCIe Block Customization**
  Illustrates customizing the PL PCIe block. You will learn how to utilize the various configuration options. {Lecture, Lab}

- **PCIe Block Test Bench and Simulation**
  Discusses PCIe block simulation. You will learn how to utilize the generated example design to verify the functionality of the PL PCIe solution. {Lecture, Lab}

Day 2

- **PCIe Block Implementation**
  Discusses implementation topics. You will review the placement recommendations for the PL PCIe blocks, transceivers, clocks, and resets. {Lecture, Lab}

- **PL PCIe Block Debugging Overview**
  Describes the PCI Express debugging options in the Versal ACAP PCI Express physical and transaction layers. You will learn how to perform PCI Express link debug. {Lecture, Lab}

- **Introduction to DMA**
  Reviews DMA basics and describes DMA in the context of the PCI Express standard. {Lecture}

- **PL PCIe XDMA/Bridge Subsystem**
  Describes the Xilinx XDMA architecture and features as well as DMA descriptor usage and interface options. You will learn how to utilize the Xilinx XDMA subsystem. {Lecture, Lab}

- **PL PCIe QDMA Subsystem**
  Describes the Xilinx QDMA architecture and features. You will learn how to utilize the Xilinx QDMA subsystem and its queue usage. {Lecture}

- **CPM4 Architecture and Functionality**
  Describes the CPM4 block architecture and functionality. You will learn the commonalities and differences to the PL PCIe solution. {Lecture}

- **CPM Block Customization**
  Reviews the configuration options of the CIPS CPM block. You will learn how to customize the CPM PCIe block. {Lecture}

- **CPM IP Use Cases**

  Describes typical use cases for the Versal ACAP PCI Express solutions to enable you to select the right solution for your design requirements. {Lecture, Lab}