Designing FPGAs Using the Vivado Design Suite 4

FPGA 4

FPGA-VDES4 (v1.0)

Course Specification

Course Description

Learn how to use the advanced aspects of the Vivado® Design Suite and Xilinx hardware.

The focus is on:

- Applying timing constraints for source-synchronous and system-synchronous interfaces
- Utilizing floorplanning techniques
- Employing advanced implementation options
- Utilizing Xilinx security features
- Identifying advanced FPGA configurations
- Debugging a design at the device startup phase
- Using Tcl scripting in non-project batch flows

This is the final course in the *Designing FPGAs Using the Vivado Design Suite* series.

What's New for 2020.1

- Design Analysis and Floorplanning: Clarification on the default Pblock type (soft) to improve design performance
- Introduction to the Xilinx XHub Stores: Additional information on the Xilinx XHub Stores

Level – FPGA 4

Course Details

- 2 days
  - 27 lectures
  - 10 labs
  - 4 demos

Price –

Course Part Number – FPGA-VDES4

Who Should Attend? – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites

- *Designing FPGAs Using the Vivado Design Suite 2* course
- *Designing FPGAs Using the Vivado Design Suite 3* course
- At least six months of design experience with Xilinx tools and FPGAs

Software Tools

- Vivado Design or System Edition 2020.1

Hardware

- Architecture: UltraScale™ family*
- Demo board: Zynq® UltraScale+™ ZCU104 board

* This course focuses on the UltraScale architecture. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Apply appropriate I/O timing constraints and design modifications for source-synchronous and system-synchronous interfaces
- Analyze a timing report to identify how to center the clock in the data eye
- Utilize floorplanning techniques to improve design performance
- Employ advanced implementation options, such as incremental compile flow, physical optimization techniques, and re-entrant mode as last mile strategies
- Utilize Xilinx security features, bitstream encryption, and authentication using AES for design and IP security
- Identify advanced FPGA configurations, such as daisy chains and gangs, for configuring multiple FPGAs in a design
- Debug a design at the device startup phase to debug issues related to startup events, such as MMCM lock and design coming out of reset
- Use Tcl scripting in non-project batch flows to synthesize, implement, and generate custom timing reports

Course Outline

Day 1

- **UltraFast Design Methodology: Design Closure**
  Introduces the UltraFast™ design methodology guidelines covered in this course. {Lecture}
- **Scripting in Vivado Design Suite Non-Project Mode**
  Write Tcl commands in the non-project batch flow for a design. {Lecture, Lab}
- **Hierarchical Design**
  Overview of the hierarchical design flows in the Vivado Design Suite. {Lecture}
- **Managing Remote IP**
  Store IP and related files remote to the current working project directory. {Lecture, Lab}
- **I/O Timing Scenarios**
  Overview of various I/O timing scenarios, such as source- and system-synchronous, direct/MMCM capture, and edge/center aligned data. {Lecture}
- **System-Synchronous I/O Timing**
  Apply I/O delay constraints and perform static timing analysis for a system-synchronous input interface. {Lecture, Demo}
- **Source-Synchronous I/O Timing**
  Apply I/O delay constraints and perform static timing analysis for a source-synchronous, double data rate (DDR) interface. {Lecture, Lab}
- **Timing Constraints Priority**
  Identify the priority of timing constraints. {Lecture}
- **Case Analysis**
  Understand how to analyze timing when using multiplexed clocks in a design. {Lecture}
- **Introduction to Floorplanning**
  Introduction to floorplanning and how to use Pblocks while floorplanning. {Lecture}
- **Design Analysis and Floorplanning**
  Explore the pre- and post-implementation design analysis features of the Vivado IDE. {Lecture, Lab}
- **Congestion**
  Identifies congestion and addresses congestion issues. {Lecture}
- **Introduction to the Xilinx XHub Stores**
  Introduces the Xilinx XHub Stores. {Lecture, Demo}
- **Incremental Compile Flow**
  Utilize the incremental compile flow when making last-minute RTL changes. {Lecture, Lab}

Day 2

- **Timing Closure Using Physical Optimization Techniques**
  Use physical optimization techniques for timing closure. {Lecture}

- **Vivado Design Suite ECO Flow**
  Use the ECO flow to make changes to a previously implemented design and apply changes to the original design. {Lecture, Lab}
- **Power Management Techniques**
  Identify techniques used for low power design. {Lecture}
- **Daisy Chains and Gangs in Configuration**
  Introduces advanced configuration schemes for multiple FPGAs. {Lecture}
- **Bitstream Security**
  Understand the Xilinx bitstream security features such as readback disable, bitstream encryption, and authentication. {Lecture, Demo}
- **Vivado Design Suite Debug Methodology**
  Understand and follow the debug core recommendations. Employ the debug methodology for debugging a design using the Vivado logic analyzer. {Lecture}
- **Trigger and Debug at Device Startup**
  Debug the events around the device startup. {Lecture, Demo}
- **Trigger Using the Trigger State Machine in the Vivado Logic Analyzer**
  Use trigger state machine code to trigger the ILA and capture data in the Vivado logic analyzer. {Lecture, Lab}
- **Debugging the Design Using Tcl Commands**
  Use Tcl scripting for VLA designs for adding probes and making connections to probes. {Lecture, Lab}
- **Using Procedures in Tcl Scripting**
  Employ procedures in Tcl scripting. {Lecture}
- **Using Lists in Tcl Scripting**
  Employ lists in Tcl scripting. {Lecture}
- **Using Regular Expressions in Tcl Scripting**
  Use regular expressions to find a pattern in a text file while scripting an action in the Vivado Design Suite. {Lecture, Lab}
- **Debugging and Error Handling in Tcl Scripts**
  Understand how to debug errors in a Tcl script. {Lecture}

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