DSP Design Using System Generator

DSP 3

DSP-SYSGEN (v1.0)

Course Specification

Course Description

Explore the Model Composer and System Generator tool and gain the expertise needed to develop advanced, low-cost DSP designs.

This course focuses on:

- Implementing DSP functions using System Generator for DSP
- Utilizing design implementation tools
- Verifying through hardware co-simulation

What's New for 2020.2

- Added Vitis™ HLS tool support for System Generator integration

Level – DSP 3

Course Duration – 2 days

Price –

Course Part Number – DSP-SYSGEN

Who Should Attend? – System engineers, system designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design

Prerequisites

- Experience with the MATLAB and Simulink software
- Basic understanding of sampling theory

Software Tools

- Vivado® Design Suite System Edition 2020.2
- Model Composer and System Generator
- Vitis HLS tool 2020.2
- Vitis unified software platform 2020.2
- MATLAB with Simulink software R2020b

Hardware

- Architecture: 7 series and UltraScale™ FPGAs
- Demo board: Kintex® UltraScale™ FPGA KCU105 board and Zynq® UltraScale+™ MPSoC ZCU104 board*

* Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations. The ZCU104 board is required for the "AXI4-Lite Interface Synthesis" lab.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Run hardware co-simulation
- Identify the high-level blocks available for FIR and FFT designs
- Implement multi-rate systems in System Generator
- Integrate System Generator models into the Vivado IDE
- Design a processor-controllable interface using System Generator for DSP
- Generate IPs from C-based design sources using the Vitis HLS tool for use in the System Generator environment
- Create and simulate designs using Model Composer

Course Outline

Day 1

- Introduction to System Generator
- Simulink Software Basics
- **Lab 1:** Using the Simulink Software
- Basic Xilinx Design Capture
- Demo: System Generator Gateway Blocks
- **Lab 2:** Getting Started with Xilinx System Generator
- Signal Routing
- **Lab 3:** Signal Routing
- Implementing System Control
- **Lab 4:** Implementing System Control

Day 2

- Multi-Rate Systems
- **Lab 5:** Designing a MAC-Based FIR
- Filter Design
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block
- System Generator, Vivado Design Suite, and Vitis HLS Integration
- **Lab 7:** System Generator and Vivado IDE Integration
- DSP Platforms
- **Lab 8:** System Generator and Vitis HLS Tool Integration
- **Lab 9:** AXI4-Lite Interface Synthesis
- Introduction to Model Composer
- Demo: Introduction to Model Composer
- [OPTIONAL]: Importing C/C++ Code to Model Composer
- [OPTIONAL]: Automatic Code Generation Using Model Composer
- [OPTIONAL]: Lab 10: Model Composer and Vivado IDE Integration

Lab Descriptions

- **Lab 1:** Using the Simulink Software – Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.
- **Lab 2:** Getting Started with Xilinx System Generator – Illustrates a DSP48-based design. Perform hardware co-simulation verification targeting a Xilinx evaluation board.
- **Lab 3:** Signal Routing – Design padding and unpadding logic by using signal routing blocks.
- **Lab 4:** Implementing System Control – Design an address generator circuit by using blocks and Mcode.
- **Lab 5:** Designing a MAC-Based FIR – Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware co-simulation by using a Xilinx evaluation board.
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block – Design a bandpass FIR filter by using the FIR Compiler block to demonstrate increased productivity. Verify the design through hardware co-simulation by using a Xilinx evaluation board.
- **Lab 7:** System Generator and Vivado IDE Integration – Embed System Generator models into the Vivado IDE.
- **Lab 8:** System Generator and Vitis HLS Tool Integration – Generate IP from a C-based design to use with System Generator.

- **Lab 9:** AXI4-Lite Interface Synthesis – Package a System Generator for DSP design with an AXI4-Lite interface and integrate this packaged IP into a Zynq UltraScale+ MPSoC processor system. Then create and debug the application project using the Vitis IDE.
- **Lab 10:** Model Composer and Vivado IDE Integration - Embed a Model Composer model into the Vivado IDE.

Register Today

Visit the Xilinx Customer Training Center to view schedules and register online.