P Series Design Environment Overview

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PCI FPGA Accelerator Card

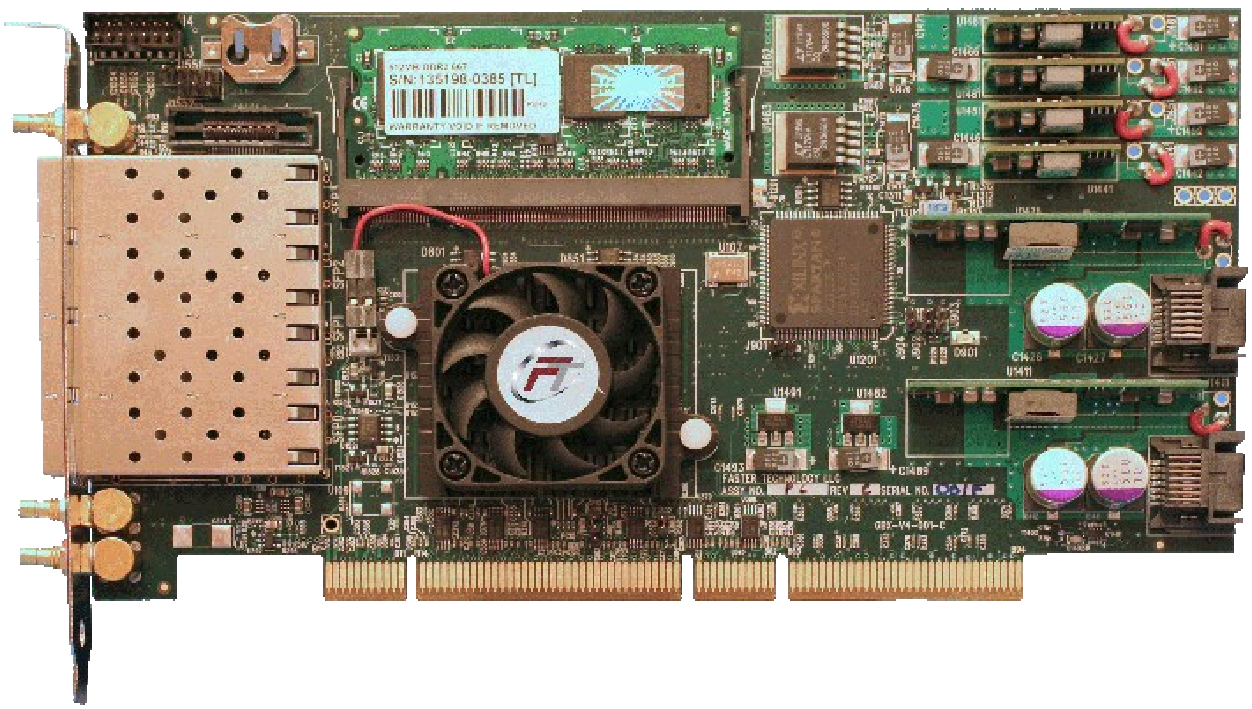

Table of Contents

1 Introduction

This document gives an overview of the design environment for the P series PCI FPGA hardware.

2 Supported tools

2.1 Xilinx EDK and ISE Foundation

The P series uses the Xilinx Embedded Development Kit (EDK) as the top level tool that assembles the FPGA design from a library of supplied cores, and any custom cores designed by the user.

FTL provides an EDK Board Support Package (BSP) that describes the P series of cards to EDK, and provides a repository of IP cores that provide the I/O interfaces for the card. In addition, a collection of building block and processing cores are provided.

EDK is based on the concept of packaged cores using standard buses as I/Os to allow the quick assembly of FGPA systems on a chip. EDK allows the user to quickly add cores to a design via a GUI. It then generates the top level VHDL code and runs the design through the synthesis and place and route back end tools.

The IBM CoreConnect family of buses are used for shared on chip buses. The Xilinx FSL bus is also supported for point to point connections. IP cores may also use ports and pins directly.

Cores in the EDK format may also have TCL scripts that are run at various points in the tool chain. FTL makes use of these scripts to automatically generate constraint files at the core level that aid the tools in achieving more repeatable results, ensure that timing constraints are met and to provide design rule checking based on how the user has configured the core in their design.

Numerous EDK reference designs for the P6 provide a functional starting point for new designs, and a demonstration of the provided cores.

2.2 Impulse C

Impulse C™ CoDeveloper software by Accelerated Impulse Technologies Inc. provides the user the ability to compile C code to VHDL or Verilog.

FTL provides a Platform Support Package that allows the CoDeveloper software to export Impulse C™ designs as EDK IP cores for use on the P6. It also exports the Linux software required to use the Impulse C core from embedded Linux programs running on the PowerPC inside the FPGA.

A variety of reference designs are provided to give the user working examples of how to use Impulse C™ with the P6.

2.3 ModelSim

EDK has the ability to export an FPGA design to an external simulator. Faster Technology has built on this to add the ability to export a board level simulation model of a user's design. FTL currently supports ModelSim PE (requiring both the VHDL and Verilog licenses and the LMC SwiftModel license). We also support the use of the code coverage license. Support for ModelSim SE is currently being evaluated.

In addition to the P6 EDK reference designs that are intended to be compiled and run on real hardware, FTL also provides a number of EDK reference designs that are verification test benches for the supplied IP cores. We make use of the IBM CoreConnect tool kit Bus Functional Models, and the ModelSim code coverage features to ensure robust verification of our IP cores.

3 Embedded Linux Environment

Faster Technology supplies a Linux distribution that runs on one of the PowerPC processors in the FPGA. It is a full version of Linux supporting virtual memory and uses the 2.4 kernel. FTL has modified the distribution to provide support for the P6, including device drivers for the I/O and processing cores that we provide.

4 Provided Cores

4.1 Board Support Core

The FTL Board Support Core with CoreSensor™ technology is an essential part of the FTL design environment. It contains TCL code that is shared by many of the other cores, and hardware that is common to most designs using the P6. The CoreSensor™ technology allows the EDK design environment to export information about the FPGA system being compiled. It also allows the Linux system running on a P6 to query for this information at run time so that one Linux build may be run on multiple FPGA builds. By decoupling the Linux and FPGA build processes CoreSensor™ technology allows software to benefit from the flexibility of the FPGA, while managing the complexity of working with reconfigurable hardware.

4.2 I/O cores

4.2.1 PLB DDR2

A custom high performance PLB to DDR2 interface is provided to support the memory centric architecture of the P6. It allows the PLB bus to achieve high efficiency by supporting its more advanced features such as simultaneous reads and writes.

4.2.2 PCI PLB OPB

The PCI core has a built in DMA engine that allows it to move data as a master on both the PLB and PCI buses. It will respond to PCI target transactions with corresponding master transactions on the OPB side.

4.2.3 DUAL PLB GigE

An embedded offload engine in the dual Gigabit Ethernet core allows selected traffic to be offloaded from the Linux network stack running on the PowerPC. The selected streams of data are sent via DMA to contiguous circular buffers in DDR2 memory. The embedded offload engine is based on the Xilinx PicoBlaze soft processor and is programed in assembly language. The program for the offload engine is loaded by the PowerPC. An offload program for the SDDS real time Signal Data Distribution System is available. The SDDS protocol is wrapped in UDP/IP and is multicast over VLANs. The availability of this offload program is subject to compliance with United States export control laws.

4.2.4 MiniSD

The miniSD card that is used to configure the Virtex-4 is also available for use by the V4 after configuration. A boot loader program is supplied that can load and run a program from the miniSD card, such as Linux. The miniSD card can also be mounted from Linux as a read/write FAT file system.

4.2.5 Serial Ports

Two serial ports are provided utilizing Xilinx serial port cores in the EDK library.

4.2.6 GPIO

The GPIO core from the Xilinx EDK library is used to provide support for the switches and LEDs.

4.2.7 SPI ROM

The SPI ROM that contains the board serial number, MAC IDs and other build information may be mounted and read by software running in the embedded Linux environment. The information in the SPI ROM is formated as an XML file.

4.2.8 Pseudo SRAM

A Xilinx memory controller core from the EDK library is used to access this memory. In systems running the embedded Linux and communicating with a system via the PCI interface, this memory is reserved for that communication.

4.3 Other cores

4.3.1 PLB to FSL IPIF

This core is designed to be a common front end to cores that process streaming data, such as many DSP cores. It provides a PLB DMA engine that understands circular buffers and is capable of performing maximum length deterministic burst transfers when combined with the FTL PLB DDR2 core.

The user side interface of this core consists of up to eight FSL buses in each direction. Each of the FSL buses has its own DMA channel, and they run independently. The PLB DMA engine is capable of performing simultaneous read and write transfers for high throughput.

4.3.2 Re-sampler

This is an asynchronous re-sampler or synchronous rate changer. An application program is available that understands the SDDS data format, and uses the meta data embedded in the data stream to control the core.

Embedded SDDS time codes are recalculated to account for the re-sampling that was performed. The availability of this application program is subject to compliance with United States export control laws.

4.3.3 DDC

This core can tune, filter and decimate a stream of data. An application program is available that understands the SDDS data format. Embedded SDDS time codes are recalculated to account for the processing. The availability of this application program is subject to compliance with United States export control laws.

4.3.4 FFT

This core performs FFTs on blocks of streaming data.

5 FTL Provided Reference Designs

Faster Technology provides a number of reference designs in support of the P6 and FTL IP cores. The reference designs serve multiple purposes.

They allow a new user to quickly go through the work flow of creating a design to get the feel of the work environment.

They allow a new user to verify that their tool set is properly installed and working.

Users can copy a reference design and use it as a starting point for a new designs.

They are used for regression testing of our releases.

The reference designs are grouped in categories.

Design names starting with “P0_” are not intended to be compiled to hardware, but are simulation reference designs. Some of these have test code running on the simulated PowerPC, and some of them use IBM bus functional models to create the test stimulus.

Designs starting with “P6_1_” are reference designs aimed at signal processing. The P6_1_1 reference design is the basis for most of the other reference designs.

Designs starting with “P6_2_” are reference designs demonstrating the use of Impulse C.

6 Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/11/2007	1.0	Initial release.
9/4/2008	1.1	Added additional details