Designing with the Virtex-4 Family

V4-23000-8-ILT (v1.0)

Course Specification

Course Description

Interested in learning how to utilize Virtex™-4 FPGA architectural resources effectively? This course focuses on understanding and utilizing several of the new and enhanced resources found in our newest device. Topics covered include an overview of the Virtex-4 FPGA; the Digital Clock Manager (DCM) and Phase-Matched Clock Divider (PMCD); global and regional clocking techniques; memory and FIFO; and source-synchronous resources. A combination of modules and labs allow for practical hands-on application of the principles taught in this course.

Level – Intermediate
Course Duration – 2 days
Price – $1200 or 12 Xilinx Training Credits
Course Part Number – V4-23000-8-ILT
Who Should Attend? – Experienced Xilinx users or those who have taken the *Fundamentals of FPGA Design* and *Designing for Performance* courses. Students should have a solid understanding of Virtex-II, Virtex-II Pro, and Virtex-II ProX FPGA architectures, the ISE™ software, timing constraints, and timing closure techniques.

Prerequisites

- *Fundamentals of FPGA Design* course
- *Designing for Performance* course
- Understanding of the Virtex-II, Virtex-II Pro, Virtex-II Pro X FPGA architecture
- Intermediate knowledge of VHDL or Verilog

Software Tools

- Xilinx ISE 8.1i
- Xilinx XST

After completing this comprehensive training, you will have the necessary skills to:

- Describe the Digital Clock Manager (DCM) and Phase-Matched Clock Divider (PMCD) functionality of the Virtex-4 FPGA
- Describe the global and regional clock resources of the Virtex-4 FPGA
- Describe the ILOGIC and OLOGIC blocks
- Describe the ISERDES and OSERDES blocks
- Describe the block RAM features in the Virtex-4 FPGA
- Describe the new FIFO-dedicated resources
- Specify the features of the DSP48 block
- Describe what's new in the configuration of the Virtex-4 FPGA

Course Outline

Day 1

- Introduction
- Product Overview
- DCM Clock Management
- PMCD Clock Management
- **Lab 1:** DCM Clocking
- Clock Networks
- **Lab 2:** Clocking Resources

Day 2

- Day Two Overview
- I/O and Source-Synchronous Resources
- **Lab 3:** Utilizing Source-Synchronous I/O Resources
- Block RAM Memory Resources
- FIFO16 Memory Resources
- **Lab 4:** Utilizing Block RAM and FIFO16
- XtremeDSP™ Technology Slice
- **Lab 5:** Utilizing XtremeDSP Technology Resources
- Configuration
- Day Two Review

Lab Descriptions

- **Lab 1:** DCM Clocking – Designing a clock management scheme with DCMs and PMCDs.
- **Lab 2:** Clocking Resources – Utilizing global and regional clock networks.
- **Lab 3:** Utilizing Source-Synchronous I/O Resources – Creating a source-synchronous design interface for a network application.
- **Lab 4:** Utilizing Block RAM and FIFO16 – Utilizing new block RAM features and FIFO16-dedicated resources.
- **Lab 5:** Utilizing XtremeDSP Technology Resources – Utilizing the DSP48 block.

Register Today

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