XILINX®

S6V6-21000-13-ILT (v1.0)

Course Specification

Course Description

Are you interested in learning how to effectively utilize Spartan®-6 or Virtex®-6 FPGA architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the *Essentials of FPGA Design* course. This course focuses on understanding as well as how to properly design for the primary resources found in these popular device families.

Topics covered include device overviews, CLB construction, DCM and PLL clocking resources, global, regional and I/O clocking techniques, memory, DSP, and source-synchronous resources. Memory controller support and the dedicated hardware resources available in each of the sub-families (EMAC, PCI Express® technology, and GTP transceivers) are also introduced.

This course also includes a detailed discussion about proper HDL coding techniques that enables designers to avoid common mistakes and get the most out of their FPGA. A combination of modules and labs allow for practical hands-on application of the principles taught.

Level – FPGA 3
Course Duration – 3 days
Price – $1800 or 18 Xilinx Training Credits
Course Part Number – S6V6-21000-13-ILT
Who Should Attend? – For those who have taken the *Essentials of FPGA Design* course
Prerequisites
- *Essentials of FPGA Design* course
- Intermediate VHDL or Verilog knowledge
Software Tool
- Xilinx ISE® Design Suite: Logic or System Edition 13.1
Hardware
- Architecture: Spartan-6 and Virtex-6 FPGAs*
- Demo board: None*

* This course focuses on the Spartan-6 and Virtex-6 architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:
- Describe all the functionality of the 6-input LUT and the CLB construction of the Spartan-6 and Virtex-6 FPGAs
- Specify the CLB resources and the available slice configurations for the Spartan-6 and Virtex-6 FPGAs
- Define the block RAM and DSP resources available for Spartan-6 and Virtex-6 FPGAs
- Properly design for the I/O block and SERDES resources
- Identify the DCM, PLL, and clock routing resources included with each of these families
- Identify the supported memory controllers for the Spartan-6 and Virtex-6 FPGAs
- Properly code your HDL to get the most out of these devices
- Describe the additional dedicated hardware for all the Spartan-6 and Virtex-6 families
- Identify the features of the 7 series families

Course Outline
Day 1
- Spartan-6 FPGA Overview
- Virtex-6 FPGA Overview
- CLB Architecture
- HDL Coding Techniques

- **Lab 1:** CLB Resources
- Memory Resources
- DSP Resources
Day 2
- **Lab 2:** DSP Resources
- Basic I/O Resources
- Spartan-6 FPGA I/O Resources
- Virtex-6 FPGA I/O Resources
- **Lab 3:** I/O Resources
- Basic Clocking Resources
Day 3
- Spartan-6 FPGA Clocking Resources
- Virtex-6 FPGA Clocking Resources
- **Lab 4:** Clocking Resources
- Memory Controllers
- Dedicated Hardware

Lab Descriptions
- **Lab 1: CLB Resources** – Using XST, synthesize a 32-bit incrementer with terminal count logic and pipelining registers. Verify that the appropriate resources were used with the RTL and technology viewers included with XST. Use the FPGA Editor to inspect the implemented results.

- **Lab 2: DSP Resources** – Using XST, synthesize and implement a wide MACC. Device usage will be verified via the FPGA Editor. Using the CORE Generator™ tool, construct, instantiate, and implement a wide pipelined multiplier. Verify the results with the FPGA Editor.

- **Lab3: I/O Resources** – Using the ISE tools, complete the construction of the transmit SERDES datapath. Explore through simulation the behavior of the various blocks. Also use the FPGA Editor to explore the physical resources of the FPGA that are used for construction of a high-speed interface.

- **Lab 4: Clocking Resources** – Using the Clocking Wizard, build and optimize the appropriate PLL, DCM, and clock routing resources. Also instantiate these resources into the design. After the design is implemented, verify hardware usage with the FPGA Editor and explore other aspects of the silicon layout.

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