TMRTool

MILAE10000-7-ILT (v1.0)

Course Specification

Course Description

This comprehensive course is a thorough introduction to the Xilinx TMR (XTMR) solution for designs that require Triple Module Redundancy. The XTMR solution incorporates TMRTool, a proprietary software application that offers total control and flexibility for the TMR process for Xilinx FPGAs.

TMRTool allows you to easily trade off maximum radiation effect immunity against area, pinout, and board layout consideration.

The XTMR solution consists of TMR and device scrubbing. This combination fully accounts for the unique programmable logic and routing resources in FPGAs, delivering maximum SEU/SET protection. This class covers all those topics.

This one-day course offers valuable hands-on experience, allowing you to evaluate TMR's timing impact, as well as area and pinout considerations. You will also perform design verification to ensure functional integrity for pre- and post-TMR circuits.

Incoming students with little knowledge of SEU/SET considerations will get a thorough overview of how these risks affect technology in general and FPGAs in particular.

Level – Fundamental to Intermediate
Course Duration – 1 day
Price – $600 or 6 Xilinx Training Credits
Course Part Number – MILAE10000-7-ILT
Who Should Attend? – Any design engineer who creates hardware with TMR requirements. This includes spaced-based deployment or similarly hostile environments
Prerequisites

- Basic digital design knowledge

Software Tools

- TMRTool 7.1
- ISE™ 7.1i
- ModelSim PE 6.0c

After completing this comprehensive training, you will have the necessary skills to:

- Recognize and address unique FPGA TMR challenges
- Perform comprehensive TMR for Xilinx FPGAs
- Prioritize SEU/SET risks against area and pinout limitations
- Incorporate device scrubbing into TMR strategy
- Create effective timing constraints for TMR design
- Modify testbenches to handle post-TMR circuits
- Incorporate TMRTool into the standard ISE design flow
- Choose the best overall solution for maximum SEU/SET immunity

Course Outline

- Virtex-II Radiation Effects Summary
- XTMR and Scrubbing Overview
- **Lab 1:** Basic TMRTool Design Flow
- XTMR and TMRTool Details
- XTMR and Timing Constraints
- **Lab 2:** Timing Constraints and Design Verification
- Performance and Application Issues
- **Lab 3:** Performance and Application Issues
- **Lab 4:** TMRTool Custom Macro Flow

Lab Description

This course is a lab-intensive, one-day workshop that gives you practical hands-on experience with TMRTool, design verification, timing constraints, and device implementation.

Each lab exercise offers insight to the underlying concepts, while enhancing designer skills and productivity. The exercises are briefly described here.

- **Lab 1:** Basic TMRTool Design Flow **–** Incorporate the TMRTool into the overall ISE design flow, set XTMR options, and export the post-TMR design
- **Lab 2:** Timing Constraints and Design Verification **–** Update timing constraints for TMR designs, modify the testbench for post-TMR design verification
- **Lab 3:** Performance and Application Issues **–** Evaluate trade-offs for output registers and bidirectional I/O, and assess impact of half-latch removal
- **Lab 4:** TMRTool Custom Macro Flow **–** Create user-defined macros as necessary for critical paths or functional blocks. Replace existing components for TMR circuit. Rerun simulation to ensure pre- and post-TMR logic and functional integrity

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