How to Design a High-Speed Memory Interface

Connectivity 3

MEM21000-14-ILT (v1.0, No Markings)

Course Specification

Course Description

This course teaches hardware designers who are new to high-speed memory I/O to design a memory interface in Xilinx FPGAs. It introduces designers to the basic concepts of high-speed memory I/O design, implementation, and debug using Xilinx 7 series FPGAs.

Additionally, students will learn about the tools available for high-speed memory interface design, debug, and implementation of high-speed memory interfaces.

The major memory types covered are DDR2 and DDR3. The following memory types are covered on demand: RLDRAMII, LPDDR, and QDRII+. Labs are available for DDR3 on the Kintex™-7 FPGA KC705 board.

Level – Connectivity 3

Course Duration – 2 days

Price – $1200 or 12 Xilinx Training Credits

Course Part Number – MEM21000-14-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- VHDL or Verilog experience or *Designing with VHDL* or *Designing with Verilog* course
- Familiarity with logic design: state machines and synchronous design
- Very helpful to have:
- Basic knowledge of FPGA architecture
- Familiarity with Xilinx implementation tools
- Nice to have:
- Familiarity with I/O basics
- Familiarity with high-speed I/O standards

Software Tools

- Xilinx ISE® Design Suite: Logic or System Edition 14.1
- Mentor HyperLynx SI

Hardware

- Architecture: 7 series FPGAs
- Demo board: Kintex-7 FPGA KC705 board

After completing this comprehensive training, you will have the necessary skills to:

- Identify the FPGA resources required for memory interfaces
- Describe different types of memories
- Utilize the Xilinx tools to generate memory interface designs
- Simulate memory interfaces with the Xilinx ISim simulator
- Implement memory interfaces
- Identify the board design options for the realization of memory interfaces
- Test and debug your memory interface design

Course Outline

Day 1

- Introduction
- 7 Series FPGAs Overview
- Memory Devices
- 7 Series FPGAs Memory Interface Resources
- Memory Controller Details and Signals
- MIG Design Generation
- **Lab 1:** MIG Core Generation

Day 2

- Memory Design Simulation
- **Lab 2:** MIG Design Simulation
- Memory Design Implementation
- **Lab 3:** MIG Design Implementation
- Memory Interface Board-Level Design
- Memory Interface Test and Debugging
- **Lab 4:** MIG Design Debugging
- Course Summary

Lab Descriptions

- **Lab 1:** MIG Core Generation – Create a DDR3 memory controller using the Memory Interface Generator (MIG) CORE Generator™ interface. Customize the soft core memory controller for the board.
- **Lab 2:** MIG Design Simulation – Simulate the memory controller created in Lab 1 using ISim.
- **Lab 3:** MIG Design Implementation – Implement the memory controller created in the previous labs. Modify constraints, synthesize, implement, create the bitstream, program the FPGA, and check the functionality.
- **Lab 4:** MIG Design Debugging – Debug the memory interface design utilizing the ChipScope Pro™ tool.

Register Today

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