Advanced FPGA Implementation

FPGA 4

FPGA33000-14-ILT (v1.0)

Course Specification

Course Description

Advanced FPGA Implementation tackles the most sophisticated aspects of the ISE® design suite and Xilinx hardware. Labs provide hands-on experience in this two-day training and cover the Xilinx Synthesis Technology (XST) tools.

This course requires the *Essentials of FPGA Design* and *Designing for Performance* courses as prerequisites. An intermediate knowledge of Verilog or VHDL is strongly recommended as is at least six months of design experience with Xilinx tools and FPGAs. The lecture material in this course covers the ISE tools and the 7 series FPGAs.

Level – FPGA 4

Course Duration – 2 days

Price – $1200 or 12 Xilinx Training Credits

Course Part Number – FPGA33000-14-ILT

Who Should Attend? – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites

- *Essentials of FPGA Design*
- *Designing for Performance*
- Intermediate knowledge of Verilog or VHDL is strongly recommended
- At least six months of design experience with Xilinx tools and FPGAs

Software Tools

- Xilinx ISE Design Suite: Logic or System Edition 14.1

Hardware

- Architecture: Xilinx 7 series FPGAs*

* This course focuses on the 7 series FPGA architectures. Check with your local Authorized Training Provider for the specifics of the in-class labs or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Create and edit a User Constraint File (UCF)
- Identify the I/O timing constraints and design modifications required for source-synchronous and system-synchronous interfaces
- Implement designs via the Tcl command line
- Use the PlanAhead™ tool to create area constraints
- Use design preservation techniques to simplify design ripple effects
- Change signals of interest in the ChipScope™ Pro tool for board-level debugging using the FPGA Editor

Course Outline

- Introduction
- **Lab 1:** Timing Closure Review
- UCF Editing
- **Lab 2:** UCF Editing
- Advanced I/O Timing
- **Lab 3:** Advanced I/O Timing
- Tcl Scripting
- **Lab 4:** Tcl Scripting
- Floorplanning an Effective Layout
- **Lab 5:** Floorplanning
- Design Preservation Techniques
- **Lab 6:** Design Preservation
- FPGA Editor: Viewing and Editing a Routed Design
- **Lab 7:** Advanced FPGA Editor

Lab Descriptions

- **Lab 1:** Timing Closure Review – Use the Constraints Editor to enter timing constraints.
- **Lab 2:** UCF Editing – Write constraints directly into a UCF file to guide the performance results of implementation.
- **Lab 3:** Advanced I/O Timing – Compose timing constraints for source-synchronous and system-synchronous I/O interfaces. Analyze the timing and determine changes to optimize the interface timing.
- **Lab 4:** Tcl Scripting – Write ISE tool control commands in Tcl script files to create a project and implement the design. Explore how the Tcl interface is integrated with the Project Navigator tool.
- **Lab 5:** Floorplanning – Implement a design by using floorplanned constraints to improve the timing results over a design without floorplanning.
- **Lab 6:** Advanced FPGA Editor – Use the FPGA Editor to view and edit a design. Rapidly locate and swap signals of interest for ChipScope Pro tool cores.

Register Today

To register for this course or to see a list of currently scheduled classes, please visit our secure **Online Store**.

To request a public or private class, inquire about course offerings, or any other specific Xilinx training needs, please contact Faster Technology through one of the following:

Web: **Request a Class**
Email: **registrar@fastertechnology.com**
Phone: 281-391-5482

As a Xilinx Authorized Training Provider (ATP), Faster Technology is the exclusive provider of Xilinx public and private courses in Texas, Louisiana, Oklahoma, Arkansas, Colorado, Utah, Montana and Wyoming.

Visit **www.FasterTechnology.com/training-courses** to see our full line of Xilinx education courses in the areas of FPGA Design, Embedded Systems Development, Connectivity, DSP Design, Languages, and CPLD Design.