Course Description
This course demonstrates how to use the ISE®, PlanAhead™, and Embedded Development Kit (EDK) software tools to construct, implement, and download a Partially Reconfigurable (PR) FPGA design. You will gain a firm understanding of PR technology and learn how successful PR designs are completed. You will also identify best design practices and understand the subtleties of the PR design flow.

This course covers both the tool flow and mechanics of successfully creating a PR design. It also describes several techniques focusing on appropriate coding styles for a PR system as well as system-level design considerations and practical applications.

Lab 2: Building an HDL ICAP Controller

Day 2
- Managing Clock Resources
- Managing Timing
- Lab 3: Partial Reconfiguration Timing Analysis and Constraints
- Embedded Environment (EDK)
- Lab 4: EDK Partial Reconfiguration
- Partial Reconfiguration Debugging
- Lab 5: ChipScope Pro Tool Partial Reconfiguration Monitoring
- PCIe Core and Partial Reconfiguration
- (Optional) Lab 6: Building a Fast Configuring PCIe System
- Course Summary

Lab Descriptions
- Lab 1: Partial Reconfiguration Flow – Illustrates the basic PlanAhead tool Partial Reconfiguration flow. At the completion of this lab, you will download partial bitstream to the ML605 board via the JTAG connection.
- Lab 2: Building an HDL ICAP State Machine – Illustrates how Platform Flash can be used to store both the initial full bitstream as well as a number of partial bitstreams and how a simple HDL state machine can load the partial bitstreams on command.
- Lab 3: Partial Reconfiguration Timing Analysis and Constraints – Shows how area groups and reconfigurable partitions affect design performance. TPSYNC is used to reduce the impact of partitioning on timing.
- Lab 4: EDK Partial Reconfiguration – Demonstrates how an embedded MicroBlaze™ processor can control a custom ICAP loader. All aspects of completing a full embedded PR design are covered, including the embedded hardware design, software development, and implementing reconfigurable partitions. This design leverages the System ACE interface to store partial bitstreams.
- Lab 5: ChipScope Pro Tool Partial Reconfiguration Monitoring – Use the ChipScope Pro tool to monitor and control which partial bitstream is loaded into the FPGA.
- Lab 6: Building a Fast Configuring PCIe System – Configure even the largest FPGA using PR-based techniques.

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