

Course Description

The Xilinx Zynq™ All Programmable System on a Chip (SoC) provides a new level of system design capabilities. This course provides experienced system architects with the knowledge to effectively architect a Zynq All Programmable SoC.

This course presents the features and benefits of the Zynq architecture for making decisions on architecting a Zynq All Programmable SoC project. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the integration of programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq All Programmable SoC.

The course also details the individual components that comprise the PS, I/O peripherals, timers, and caching, as well as the DMA, interrupt, and memory controllers. Emphasis will be placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL.

Level – Embedded Architect 3

Course Duration – 2 days

Price – \$1200 or 12 Xilinx Training Credits

Course Part Number – EMBD24000-14-ILT

Who Should Attend? – System architects who are interested in architecting a system on a chip using the Zynq All Programmable SoC.

Prerequisites

- Digital system architecture design experience
- Basic understanding of microprocessor architecture
- Basic understanding of C programming
- Basic HDL modeling experience

Software Tools

- Xilinx ISE Design Suite: Embedded or System Edition 14.2

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or Zed board*

* This course focuses on the Zynq-7000 All Programmable SoC. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq All Programmable SoC
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Course Outline

Day 1

- Zynq All Programmable SoC Architecture Overview
- Inside the Application Processor Unit (APU)
- Processor Input/Output Peripherals
- **Lab 1:** Building a Zynq System on a Chip
- Zynq System Architecture Essentials

- Introduction to AXI
- Zynq All Programmable SoC PS/PL AXI Ports
- **Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC

Day 2

- Zynq Device Configuration
- Zynq All Programmable SoC Memory Resources
- Zynq All Programmable SoC PL Design Architecture
- Meeting Performance Goals
- **Lab 3:** Using DMA on the Zynq All Programmable SoC
- Zynq All Programmable SoC Software Design
- Debugging the Zynq All Programmable SoC
- **Lab 4:** Debugging on the All Programmable SoC
- Zynq All Programmable SoC Tools and Reference Designs
- **Lab 5:** Running and Debugging a Linux Application on the Zynq All Programmable SoC

Lab Descriptions

- **Lab 1:** Building a Zynq System on a Chip – Examine the process of using the PlanAhead™ and Xilinx Platform Studio (XPS) tools to create a simple processing system.
- **Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC – Connect a programmable logic (PL) design to the embedded processing system (PS).
- **Lab 3:** Using DMA on the Zynq All Programmable SoC – Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.
- **Lab 4:** Debugging on the Zynq All Programmable SoC – Evaluate debugging the hardware and software components of a Zynq All Programmable SoC design.
- **Lab 5:** Running Linux on the Zynq All Programmable SoC – Explore a software application executing under the Linux operating system on the Zynq All Programmable SoC.

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