Designing with Ethernet MAC Controllers

Connectivity 3

EMAC23000-13-ILT (v1.0)

Course Specification

Course Description

Become acquainted with the various solutions that Xilinx offers for Ethernet connectivity. Learn the basics of the Ethernet standard, protocol, and OSI model while applying Xilinx solutions via hands-on laboratory exercises. Perform simulation to understand fundamental principles and obtain the knowledge to assess hardware design considerations and software development requirements.

Level – Connectivity 3

Course Duration – 2 days

Price – $1200 or 12 Xilinx Training Credits

Course Part Number – EMAC23000-13-ILT

Who Should Attend? – Engineers who would like to come up to speed on utilizing Xilinx Ethernet connectivity solutions (soft cores and hard IP)

Prerequisites

- *Essentials of FPGA Design* course
- C programming knowledge recommended
- Experience with the Xilinx ISE® and Embedded Development Kit (EDK) software tools

Software Tools

- Xilinx ISE Design Suite: System Edition 13.3
- Mentor Graphics ModelSim SE 10.0b

Hardware

- Architecture: Kintex™-7, Spartan®-6 and Virtex®-6 FPGAs*
- Demo board: Spartan-6 FPGA SP605 or Virtex-6 FPGA ML605 board*

* This course focuses on the Kintex-7, Spartan-6, and Virtex-6 architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the basics of Ethernet standard, protocol, and OSI model
- Identify the various solutions that Xilinx offers for Ethernet connectivity
- Utilize various Ethernet cores either in a standalone mode or as a peripheral in a processor-based design
- Determine an appropriate core to use
- Develop software to drive the core and achieve desired functionality
- Integrate hard and soft IP into the EDK

Course Outline

Day 1

- Ethernet Basics
- Network Protocols, Ethernet Interfaces, and Hardware
- **Lab 1:** Analyzing Ethernet Frames
- Physical Layer
- LocalLink Interface
- **Lab 2:** VLAN and Jumbo Frames
- Xilinx EMAC Solutions

Day 2

- **Lab 3:** Implementation
- 10/100 EMAC Solutions
- **Lab 4:** EMAC Peripheral in Loopback Mode
- TEMAC
- **Lab 5:** TEMAC Peripheral in Loopback Mode
- 10GE MAC
- **Lab 6:** Analyzing 10GE MAC Frames

Lab Descriptions

- **Lab 1:** Analyzing Ethernet Frames – Perform a functional simulation of a Tri-Mode EMAC core using either ISim or ModelSim. Identify the components of a Gigabit Ethernet frame. Observe how the core behaves when source and destination addresses are changed.
- **Lab 2:** VLAN and Jumbo Frames – Analyze the transmission and reception of VLAN and jumbo frames using either ISim or ModelSim. Adjust the interframe gap value and see its effect on transmission frames. View TX_STATISTICS_VECTOR and RX_STATISTICS_VECTOR and identify their contents. Study the reception of good and bad frames and their associated signals. Analyze received jumbo frames. Analyze the management interface for the configuration registers.
- **Lab 3:** Implementation – Generate a Tri-Mode Ethernet MAC core by using the CORE Generator™ tool. Synthesize a core by using the XST synthesis tool via a script file generated by the CORE Generator. Implement the core using a script file. Identify what is being generated and analyze the results.
- **Lab 4:** EMAC Peripheral in Loopback Mode – Use XPS to create a processor system. Include an AXI 10/100 EMAC peripheral in simple non-DMA mode. Program a peripheral in loopback mode.
- **Lab 5:** TEMAC Peripheral in Loopback Mode – Create a processor system, including a hard TEMAC instance to the project. Program a peripheral in loopback mode. Verify the design by generating and downloading a bitstream on either the SP605 or ML605 board.
- **Lab 6:** Analyzing 10GE MAC Frames – Perform a functional simulation of a 10-Gigabit Ethernet MAC core. Analyze RX SGMII, TX GMII, RX client data, and TX client data.

Register Today

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