How to Design a Xilinx Connectivity System in 1 Day

Connectivity 2

CONN13000-13-ILT (v1.0)

Course Specification

Course Description

This workshop introduces you to fundamental connectivity concepts and techniques for implementation in Xilinx FPGAs. The focus is on fundamental aspects of transceivers, PCIe® technology, memory interfaces, and Ethernet MACs.

Only essential theory is introduced in order to lay a foundation for the material and topics covered in this workshop, which complements more detailed training found in subsequent Xilinx courses.

Design examples and labs are drawn from the Connectivity Targeted Reference Design (TRD). In addition, an IBERT lab is available that highlights use of the MGT.

Level – Connectivity 2
Course Duration – 1 day
Price – $600 or 6 Xilinx Training Credits
Course Part Number – CONN13000-13-ILT
Who Should Attend? – FPGA designers and logic designers
Prerequisites

- VHDL or Verilog experience or *Designing with VHDL* or *Designing with Verilog* course
- FPGA design experience or *Essentials of FPGA Design* course
- Basic understanding of digital and analog circuit design
- Basic understanding of high-speed serial I/O applications

Software Tools

- Xilinx ISE® Design Suite: Logic or System Edition 13.1

Hardware

- Architecture: Spartan®-6 and Virte®x-6 FPGAs*
- Demo board: Spartan-6 FPGA SP605 or Virtex-6 FPGA ML605 board*

* This workshop focuses on the Spartan-6 and Virtex-6 architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the basic functionality and usage of connectivity hard IP
- Describe the basic functionality and usage of connectivity soft IP
- Describe the basic building blocks of the Connectivity Targeted Reference Design
- Apply your knowledge to use the Targeted Reference Design
- Apply your knowledge to modify the Targeted Reference Design for re-use in your own design
- Optimize serial links using the IBERT design

Course Outline

- Introduction
- Transceiver Overview
- **Lab 1:** GTP or GTX Core Generation
- PCI Express Technology Overview
- **Lab 2:** PCIe Core Generation
- Memory Interfaces Overview
- **Lab 3:** Memory Interface Design
- Ethernet MAC Overview
- **Lab 4:** TEMAC Design
- AXI IP Interface Overview
- Connectivity Targeted Reference Design Overview
- **Lab 5:** IBERT Lab

Lab Descriptions

- **Lab 1:** GTP or GTX Core Generation – Use the GTP/GTX Transceiver Wizard to create the transceiver core.
- **Lab 2:** PCIe Core Generation – Introduces the CORE Generator™ interface for generating the PCIe core for the Spartan-6 or Virtex-6 FPGA.
- **Lab 3:** Memory Interface Design – Create a DDR3 memory controller with the Memory Interface Generator (MIG) CORE Generator interface that will be used in a pre-written design. Download onto the development board to verify functionality.
- **Lab 4:** TEMAC Design – Use the CORE Generator interface to generate a Tri-Mode Ethernet MAC core.
- **Lab 5:** IBERT Lab – Use the ChipScope™ Pro tool IBERT design to verify a GTP link on the Spartan-6 SP605 board or a GTX link on the Virtex-6 ML605 board.

Register Today

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