XILINX

Xilinx Partial Reconfiguration Tools and Techniques
FPGA 4

Course Description

Learn how to construct, implement, and download a Partially Reconfigurable (PR) FPGA design using the Vivado® Design Suite. This course covers both the tool flow and mechanics of successfully creating a PR design.

The emphasis is on:

- Identifying best design practices and understanding the subtleties of the PR design flow
- Using the PR controller and PR decoupler IP in the PR process
- Implementing PR in an embedded system environment
- Applying appropriate debugging techniques on PR designs
- Employing best practice coding styles for a PR system

Level – FPGA 4

Course Duration – 2 days

Price –

Course Part Number – FPGA-PR

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and the Xilinx design methodology and who have need of partial reconfiguration techniques

Prerequisites

- *Designing FPGAs with the Vivado Design Suite 2* course
- *Designing FPGAs with the Vivado Design Suite 3* course
- *Designing FPGAs with the Vivado Design Suite 4* course
- Working HDL knowledge (VHDL or Verilog)

Software Tools

- Vivado Design or System Edition 2019.1

Hardware

- Architecture: UltraScale and 7 series FPGAs*
- Demo board: Kintex® UltraScale FPGA KCU105 board, Kintex-7 FPGA KC705 board, and ZedBoard**

* This course focuses on the UltraScale and 7 series architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

** The UltraScale architecture versions of the "Using the PRC IP in a Partial Reconfiguration Design" lab and the "Using ILA Cores to Debug Partial Reconfiguration Designs" lab are not available because of QSPI and PRC issues on the KCU105 board. These two labs support only the 7 series architecture. The "Partial Reconfiguration in Embedded Systems" lab requires a ZedBoard for implementation.

After completing this comprehensive training, you will have the necessary skills to:

- Build and assemble a Partially Reconfigurable system (UltraScale, 7 series, and Zynq® devices)
- Define PR regions and reconfigurable modules with the Vivado Design Suite
- Generate the appropriate full and partial bitstreams for a PR design
- Use the ICAP and PCAP components to deliver the partially reconfigurable systems
- Identify how Partial Reconfiguration affects various silicon resources, including block RAM, IOBs, fabric, clock buffers, and MGTs
- Implement a Partial Reconfiguration system using the following techniques:
  - Direct JTAG connection

Course Specification

  - Floorplanning
  - Timing constraints and analysis
- Implement a PR system using the PRC IP
- Implement a PR system in an embedded environment
- Debug PR designs

Course Outline

Day 1

- Introduction to Partial Reconfiguration
- **Demo:** Introduction to Partial Reconfiguration
- Partial Reconfiguration Flow
- **Lab 1:** Partial Reconfiguration Tool Flow
- **Lab 2:** Partial Reconfiguration Project Flow
- **Lab 3:** Floorplanning the PR Design
- Partial Reconfiguration Design Considerations
- Optional: FPGA Configuration Overview
- Partial Reconfiguration Bitstreams
- **Demo:** Partial Reconfiguration Controller (PRC) IP
- **Lab 4:** Using the Partial Reconfiguration Controller in a PR Design

Day 2

- Partial Reconfiguration: Managing Timing
- **Lab 5:** Partial Reconfiguration Timing Analysis and Constraints
- Partial Reconfiguration in Embedded Systems
- **Lab 6:** Partial Reconfiguration in Embedded Systems
- Debugging Partial Reconfiguration Designs
- **Lab 7:** Debugging a Partial Reconfiguration Design
- Partial Reconfiguration Design Recommendations
- PCIe Core and Partial Reconfiguration

Lab Descriptions

- **Lab 1:** Partial Reconfiguration Tool Flow – Illustrates the basic Vivado Design Suite Partial Reconfiguration flow. At the completion of this lab, you will download a partial bitstream to the demo board via the JTAG connection.
- **Lab 2:** Partial Reconfiguration Project Flow – Illustrates Partial Reconfiguration (PR) project flow in the Vivado® Design Suite. At the end of this lab, you will be able to create multiple RMs and configurations using Partial Reconfiguration Wizard.
- **Lab 3:** Floorplanning the PR Design – Illustrates how to create efficient Pblocks for a Partial Reconfiguration design. At the end of this lab, you will understand the impact of the SNAPPING_MODE property for a Pblock.
- **Lab 4**: Using the Partial Reconfiguration Controller in a PR Design – Illustrates using the PRC IP and hardware triggers to manage partial bitstreams.
- **Lab 5:** Partial Reconfiguration Timing Analysis and Constraints – Shows how area groups and Reconfigurable Partitions affect design performance.
- **Lab 6**: Partial Reconfiguration in Embedded Systems – Illustrates implementing PR designs in an embedded environment.
- **Lab 7**: Debugging a Partial Reconfiguration Design – Demonstrates using ILA cores to debug PR designs and shows which signals to monitor during debugging.

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Course Specification
www.xilinx.com
1-800-255-7778

Register Today

Visit the Xilinx Customer Training Center to view schedules and register online.