Course Description
This course tackles the most sophisticated aspects of the Vivado Design Suite and Xilinx hardware. Learn to utilize advanced static timing analysis and apply constraints for source-synchronous and system-synchronous interfaces. Utilize floorplanning techniques to improve design performance. Learn to use Tcl scripting in the Vivado Design Suite.

Level – FPGA 4
Course Duration – 1 day
Price – $600 or 6 Xilinx Training Credits

Course Part Number –

Who Should Attend? – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites
- Essentials of FPGA Design
- Designing for Performance
- Intermediate knowledge of Verilog or VHDL is strongly recommended
- At least six months of design experience with Xilinx tools and FPGAs

Software Tools
- Xilinx Vivado Design Suite System Edition 2012.2

Hardware
- Architecture: 7 series*
- Demo board: KC705*

* This course focuses on the 7 series architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:
- Use some of the advanced timing report features to build customized timing reports
- Describe all report timing options
- Identify the input and output timing constraints and design modifications required for source-synchronous and system-synchronous interfaces
- Use Vivado to appropriately floorplan your design and improve and preserve performance
- Implement designs via the Tcl command line

Course Outline
- Introduction
- Advanced Timing Analysis
- Lab 1: Advanced Static Timing Analysis
- Designing I/O Interface Constraints
- Lab 2: Designing I/O Interfaces
- Introduction to Pblocks
- Floorplanning Techniques
- Lab 3: Design Analysis and Floorplanning
- Scripting in the Project Based Flow
- Scripting in the Project-less Flow
- Lab 4a: Scripting in the Project Based Flow
- Lab 4b: Scripting in the Project-less Flow

Lab Descriptions
- Lab 1: Exploration of available reporting options utilizing interactive Tcl commands.
- Lab 2: Apply advanced input and output constraint on source-synchronous and system-synchronous design and validate results
- Lab 3: Floorplan your design and evaluate the floorplanning capabilities and results.
- Lab 4 (a and b): Write a script to load the design, add constraints, set properties, run synthesis and implementation, and create reports.

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