Designing with SystemVerilog

FPGA 1

LANG-SVDES (v1.0)

Course Specification

Course Description

This course provides a thorough introduction to SystemVerilog constructs for design.

This focus is on:

- Writing RTL code using the new constructs available in SystemVerilog
- Reviewing new data types, structs, unions, arrays, procedural blocks, re-usable tasks, functions, and packages
- Targeting and optimizing Xilinx devices using SystemVerilog

What's New for 2021.1

- All labs have been updated to the latest software versions

Level – FPGA 1

Course Details

- 2 days
- 16 lectures
- 6 labs

Price –

Course Part Number – LANG-SVDES

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- Verilog design experience or completion of *Designing with Verilog*

Software Tools

- Vivado® Design Suite 2021.1
- Questa Sim Prime Simulator 2019.4

Hardware

- Architecture: N/A*
- Demo board: Kintex® UltraScale™ FPGA KCU105 board*

* This course does not focus on any particular architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the features and benefits of using SystemVerilog for RTL design
- Identify the new data types supported in SystemVerilog
- Use an enumerated data type for coding a finite state machine (FSM)
- Explain how to use structures, unions, and arrays
- Describe the new procedural blocks and analyze the affected synthesis results
- Define the enhancements and ability to reuse tasks, functions, and packages
- Identify how to simplify module definitions and instantiations using interfaces
- Examine how to efficiently code in SystemVerilog for FPGA design simulation and synthesis
- Target and optimize Xilinx FPGAs by using SystemVerilog
- Synthesize and analyze SystemVerilog designs with the Vivado Design Suite
- Download a complete SystemVerilog design to an evaluation board

Course Outline

Day 1

- **Introduction to SystemVerilog**
  Provides an introduction to the SystemVerilog language. {Lecture}
- **Data Types**
  Describes the data types supported by SystemVerilog. {Lecture, Lab, Demo}
- **User-Defined and Enumerated Data Types**
  Describes user-defined and enumerated data types supported by SystemVerilog. {Lecture}
- **Type Casting**
  Describes type casting in SystemVerilog. {Lecture}
- **Arrays and Strings**
  Explains the use of arrays in SystemVerilog. {Lecture}
- **SystemVerilog Building Blocks**
  Describes the design and verification building blocks in SystemVerilog. {Lecture}
- **Structures**
  Explains the use of structures in SystemVerilog. {Lecture, Lab}
- **Unions**
  Explains the use of unions in SystemVerilog. {Lecture, Lab}
- **Additional Operators in SystemVerilog**
  Describes the operators supported by SystemVerilog beyond those found in Verilog. {Lecture}

Day 2

- **Procedural Statements**
  Describes the different procedural blocks provided by SystemVerilog. {Lecture, Lab}
- **Control Flow Statements**
  Describes the different control statements provided by SystemVerilog. {Lecture}
- **Functions**
  Explains the SystemVerilog enhancements to functions. {Lecture}
- **Tasks**
  Describes the task SystemVerilog construct. {Lecture}
- **Packages**
  Describes the package SystemVerilog construct. {Lecture, Lab}
- **Interfaces**
  Describes the concept of interfaces in SystemVerilog. {Lecture}
- **Targeting Xilinx FPGAs**
  Focuses on Xilinx-specific implementation and chip-level optimization. {Lecture, Lab}

Register Today

Visit the Xilinx Customer Training Center to view schedules and register online.