Course Description
Learn how to implement a Xilinx PCI Express® core in custom applications to improve time to market with the PCIe® core design. The focus is on:
- Constructing a Xilinx PCI Express system within the customer education reference design
- Enumerating various Xilinx PCI Express core products
- Identifying the advanced capabilities of the PCIe specification

This course also focuses on the AXI Streaming interconnect.

Level – Connectivity 3
Course Duration – 2 days
Price –
Course Part Number – CONN-PCIE
Who Should Attend?
- Hardware designers who want to create applications using Xilinx IP cores for PCI Express
- Software engineers who want to understand the deeper workings of the Xilinx PCI Express solution
- System architects who want to leverage key Xilinx advantages related to performance, latency, and bandwidth in PCI Express applications

Prerequisites
- Experience with PCIe specification protocol
- Knowledge of VHDL or Verilog
- Some experience with Xilinx implementation tools
- Some experience with a simulation tool, preferably the Vivado® simulator
- Moderate digital design experience

Software Tools
- Vivado Design or System Edition 2018.3

Hardware
- Architecture: UltraScale™ and UltraScale+™ FPGAs
- Demo board: Kintex® UltraScale FPGA KCU105 board

* This course focuses on the UltraScale and UltraScale+ architectures. Check with your local Authorized Training Provider for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:
- Construct a basic PCIe system by:
  - Selecting the appropriate core for your application
  - Specifying requirements of an endpoint application
  - Connecting this endpoint with the core
  - Utilizing FPGA resources to support the core
  - Simulating the design
- Identify the advanced capabilities of the PCIe specification protocol and feature set

Course Outline
Day 1
- Course Introduction
- Xilinx PCI Express Solutions
- Connecting Logic to the Core
- PCIe Core Customization
- Lab 1: Constructing the PCIe Core

Day 2
- Application Focus: DMA
- Lab 4: Exploring Xilinx DMA
- Design Implementation and PCIe Configuration
- Lab 5: Implementing the PCIe Design
- Root Port Applications
- Debugging and Compliance
- Lab 6: Debugging the PCIe Design
- Interrupts and Error Management
- Course Summary

Lab Descriptions
- Lab 1: Constructing the PCIe Core – This lab familiarizes you with the necessary flow for generating a Xilinx Integrated PCI Express Endpoint core from the IP catalog. You will select appropriate parameters and create the PCIe core used throughout the labs.
- Lab 2: Simulating the PCIe Core – This lab demonstrates the timing and behavior of a typical link negotiation using the Vivado simulator. You will observe and capture transaction layer packets.
- Lab 3: Using the PCI Express Core in IP Integrator – This lab familiarizes you with all the necessary steps and recommended settings to use the PCIe solutions in an IP integrator block design.
- Lab 4: Exploring the Xilinx DMA – This lab familiarizes you with all the necessary steps to set up and perform DMA transfers.
- Lab 5: Implementing the PCIe Design – This lab familiarizes you with all the necessary steps and recommended settings to turn the HDL source to a bitstream by using the Tandem configuration mode.
- Lab 6: Debugging the PCIe Design – This lab illustrates how to use the Vivado logic analyzer to monitor the behavior of the core and a small endpoint application for proper operation.

Register Today
Visit the Xilinx Customer Training Center to view schedules and register online.

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